乐升半导体
LEVETOP

LT7589

High Performance Uart TFT Display Controller

Specification

V1.2

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Version History

Version	Release Date	Description
V1.0	2024/11/22	● LT7589 Preliminary Release
V1.1	2025/03/20	● Update Pin - VDD33_IO Description ● Update Application Circuit
V1.2	2025/04/21	● Modify the pin signal description of "LCD_XI" ● Update Table 6-4 External Flash Signal Description ● Update Application Circuit

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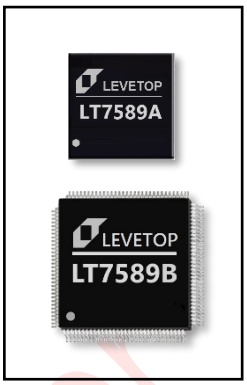
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1. Chip Introduction

1.1. Basic Introduction



LT7589 is a high-performance Serial Uart TFT Panel Controller. Internally integrated with a 32-bit RISC MCU and a GUI (Graphic User Interface) with TFT LCD graphics display controller, the main function is to provide Uart serial communication, allowing the main control MCU to easily present the information to be displayed on the TFT panel through simple serial commands. The internal hardware of LT7589 also provides JPG image decoding PIP (Picture-in-Picture), Geometric drawing and other functions can improve the display efficiency of TFT panel and reduce the time required for MCU to process graphic displays. The LT7589 supports display resolutions ranging from 480*480 (QVGA) to 1280 * 800, suitable for 16/24bit RGB interface TFT displays.

The internal MCU of LT7589 has a maximum clock frequency of 200MHz, contains 2MB Flash, 768KB SRAM, 16MB display memory, and is combined with JPG decoder, 2D graphics acceleration display, DMA data reading, and high-speed QSPI Flash interface to quickly read images, animations, word libraries, and other information stored in external QSPI Flash, with good display performance. LT7589 can be used in conjunction with UI editing software (UI-Editor) and simulation software (UI-Emulator) developed by Levetop Semiconductor to directly import and develop display interfaces for designed UI materials and display interaction logic on a computer. Its supported display functions include image display, animation display, sliding menu display, progress bar display, string display, Chinese English keyboard, numeric keyboard, analog clock, digital clock, pointer display, QR code generation, multi language, audio playback, variable control, and control effects combined with touch screen or encoder functions. In addition to the serial port screen Uart communication interface, LT7589 also provides multiple sets of SCI (Uart) interfaces to connect components such as Bluetooth modules, WiFi modules, etc. It also offers CanBus, SD card (SPI mode), analog input AIN, PWM, and INT interrupt interfaces, and comes with an RTC clock. It can also be used for GUI graphic development in Little VGL, with good fluency and high cost-effectiveness.

Due to its high capacity of Flash and SRAM, the LT7589 can also be used as a main control MCU with a TFT controller, completing the main control and TFT display functions with one LT7589. Its display function is very suitable for electronic products with TFT-LCD panels below 1280x800 resolution, or to replace the original monochrome panel products, enhancing the product's intelligent display of information, increasing product quality and grade. The powerful display function of LT7589 is very suitable for use in electronic products with TFT-LCD panels, such as various smart home appliances, car dashboards, motorcycle panels, multifunctional transaction machines, industrial controls, electronic instruments, medical beauty equipment, testing equipment, charging equipment, inverters, UPS and other power equipment, audio equipment, as well as smart speakers with TFT panel, robots and other products.

1.2. Application Block Diagram

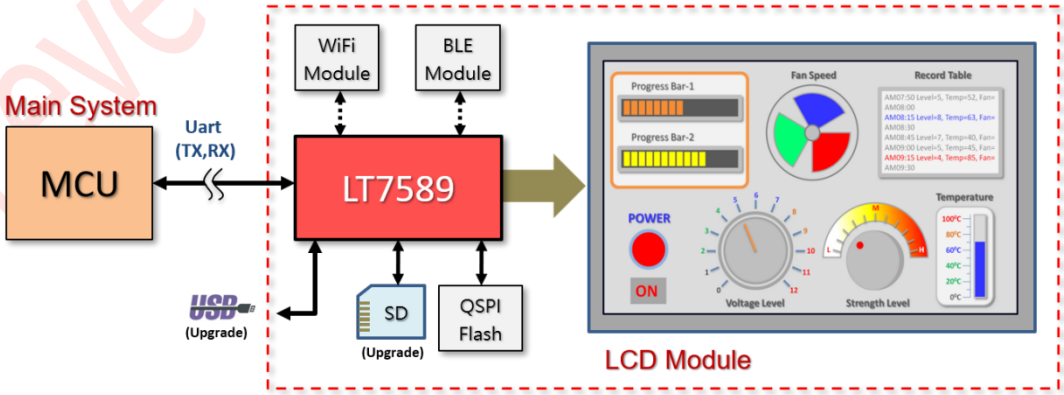


Figure 1-1: LT7589 Designed on TFT Module

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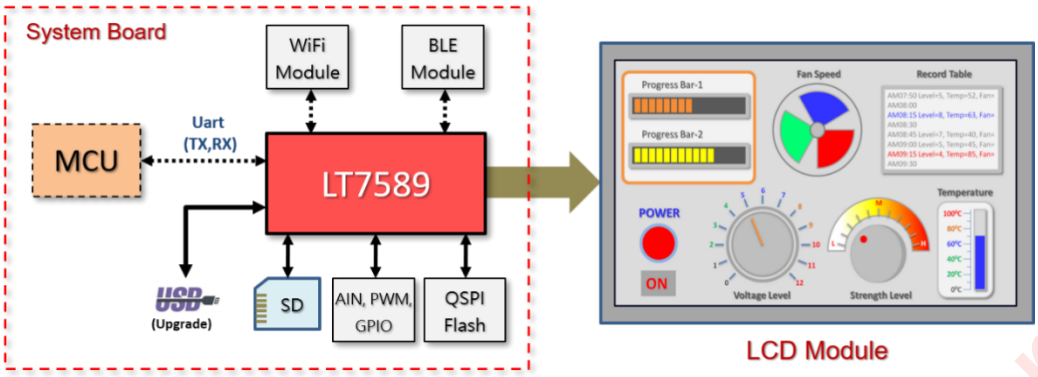


Figure 1-2: LT7589 Designed on System Board

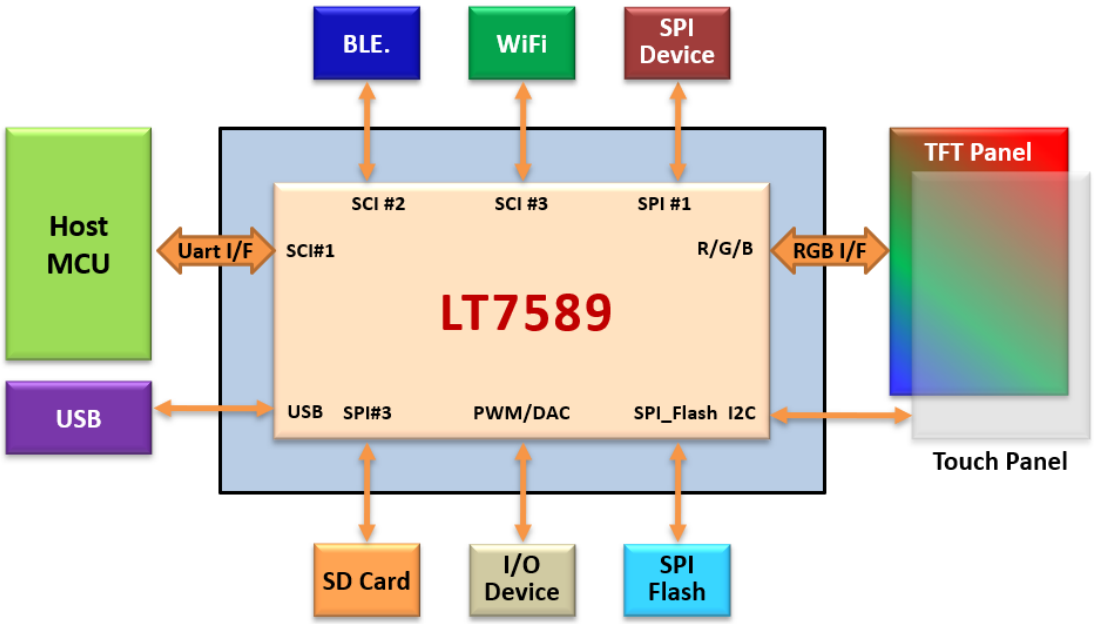


Figure 1-3: LT7589 Application Architecture

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1.3. Internal Block Diagram

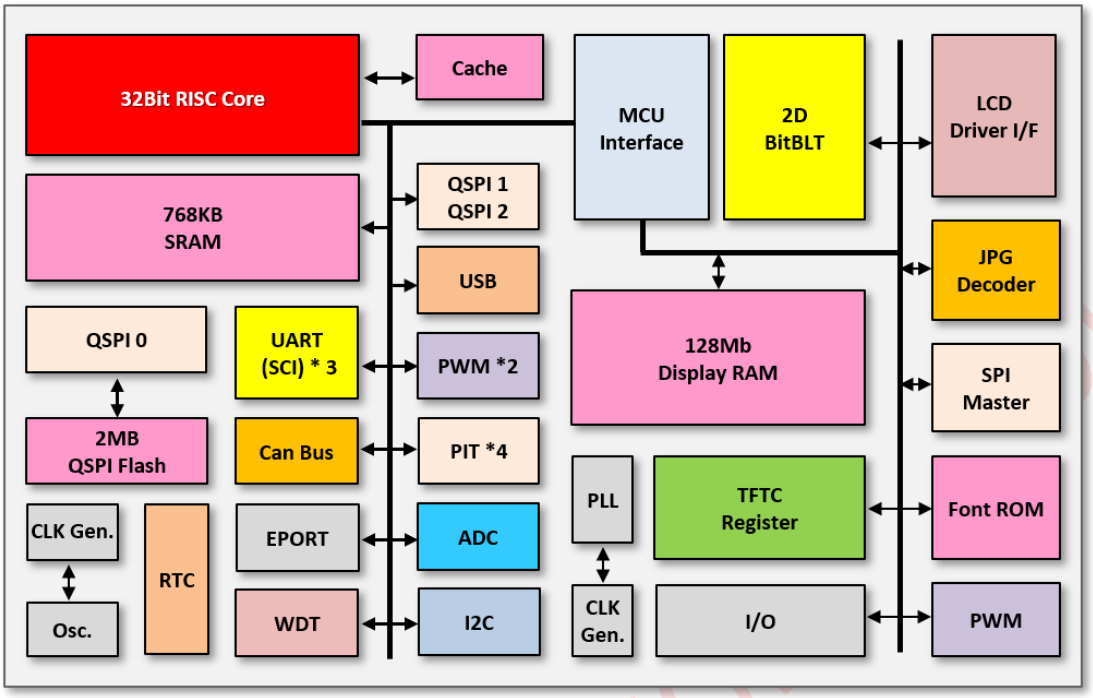


Figure 1-4: LT7589 Internal Block Diagram

Table 1-1: Part Number

Model	Package	Display RAM	Resolution	Colors
LT7589A	QFN-96	128Mb	1280*800	16.7M Color αRGB 8:8:8:8
LT7589B	LQFP-128	128Mb	1280*800	16.7M Color αRGB 8:8:8:8

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1.4. Features

Host MCU Interface

- Support Uart, USB Interface
- Embedded 32Bit MCU, main clock is 180MHz, and 200MHz for max.

USB Interface

- Support USB2.0 Full Speed。

SCI (Uart) Interface

- Supports Three SCI (Serial Communications Interface)
- Components or modules that can be connected to external SCI interfaces

Memory

- MCU Embedded 2M bytes Flash
- MCU Embedded 512K+256K bytes SRAM
- TFT Controller Embedded 128Mbit Display RAM

Display Data Format

- 16bpp : Color RGB 5:6:5 (2bytes/pixel)
- 24bpp : Color RGB 8:8:8 (3bytes/pixel)
  - αRGB 4:4:4:4 (4,096 Index color/pixel, including transparency attribute)
- 32bpp : Color αRGB 8:8:8:8 (4bytes/pixel)

Panel Interface and Resolution

- Supports 16 or 24bits RGB Interface Panel
- Supported resolutions for bare metal development:
  - VGA : 640*480 TFT Panel
  - WVGA : 800*480 TFT Panel
  - SVGA : 800*600 TFT Panel
  - XGA : 1024*768 TFT Panel
  - SXGA : 1280*1024 TFT Panel
- Maximum resolution supported during serial TFT panel development: 1280*800

Geometry Display accelerator

- Provide drawing functions such as drawing points, lines, curves, ellipses, triangles, rectangles, rounded rectangles, etc

Display Functions

- Built in JPG hardware decoder
- Support users to define four 32*32 graphic cursor options.
- Provide virtual display function: Virtual display can display images larger than the size of the LCD panel, so that the images can easily scroll in any direction.
- Provide Picture in Picture (PIP) display: Supports two PIP window regions: the enabled PIP window is displayed above the main window, while the PIP1 window is displayed above the PIP2 window.
- Support multiple display functions: You can switch the main display window between display buffers to achieve simple animation display effects.
- Support the function of quickly displaying images when awakened.
- Supports mirroring and vertical flipping display functions.
- Color Bar Display: It can still be displayed in ribbon format without writing data to the internal display memory, with a default resolution of 640 * 480 pixels.

BitBLT Engine

- Built in 2D BitBLT engine.
- Provide the function of copying images with raster operation.
- Provide color depth conversion.
- Solid filling and pattern filling functions:
  - Provide user-defined 8*8 images or 16*16 images.
- Provide the function of combining two images into one image:
  - Chroma Keying function: Mix the image with specified RGB colors based on transparency
  - Window Alpha blending mode: Mix two images based on the transparency within the specified area.
  - Pixel blending transparency mode (Dot Alpha blending): Mix two images based on RGB format and transparency.

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Display Text Mode

- Built in ISO/IEC 8859-1/2/4/5 font sizes of 8*16, 12*24, and 16*32
- Support users to customize half shaped character angles and full shaped characters (8*16, 12*24, 16*32, 16*16, 32*32).
- Supports full font sizes of 48*48 and 72*72
- Provide programmable text cursor.
- Supports vertical and horizontal font enlargement (*1, *2, *3, *4x).
- Supports 90 degree rotation of text

SPI Master Interface

- The TFT graphics accelerator provides external serial flash data copying to the frame buffer.
- Compatible with standard QSPI specifications NOR/NAND Flash.
- Support bad block handling in Nand Flash.
- Support MCU to use Pass Mode for SPI Flash.
- Provide 16 bytes read FIFO and 16 bytes write FIFO.
- When the Tx FIFO is completely cleared and the SPI Tx/Rx engine is idle, an interrupt will be issued.
- Provide 2 additional sets of compatible standard SPI interfaces.

I2C Interface

- MCU provides I2C interface to connect with external I2C devices
- Provide standard transmission mode (100kbps) and fast transmission mode (400kbps)

PWM Interface

- MCU provides 8 PWM interfaces
- The TFT controller has two built-in 16bit counters and provides two PWM output interfaces
- Programmable operation cycle

Interrupt Signals

- MCU can provide up to 19 interrupt input
- The TFT controller provides an interrupt output interface.

GPIO

- MCU can provide up to 24 GPIO Port
- The TFT controller can provide up to 17 GPIO Port

Analog Input

- MCU Supports eight ADC Analog Input

Reset

- MCU provides power on reset, external reset input, software reset, watchdog reset, and voltage detection reset
- The TFT controller provides power on reset, external hardware reset, and software command reset

Power Saving Mode

- Support Standby mode, Suspend mode and Sleep Mode
- Support MCU wake up

Clock

- MCU and TFT controller have independent clocks.
- MCU built-in precise high-frequency clock
- Built in RTC and external 32KHz crystal oscillator circuit.
- TFT controller with built-in programmable PLL, providing internal clock, external LCD clock, and internal display memory clock

Power Supply

- VDD Power: 3.3V +/- 0.3V
- Embedded 1.2V LDO

Package Type

- QFN-96Pin (10*10mm^2)
- LQFP-128Pin (14*14mm^2)

Operation Temp.

- -40℃~85℃。(@180MHz)

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2. Pin Description

2.1. Pin Assignment

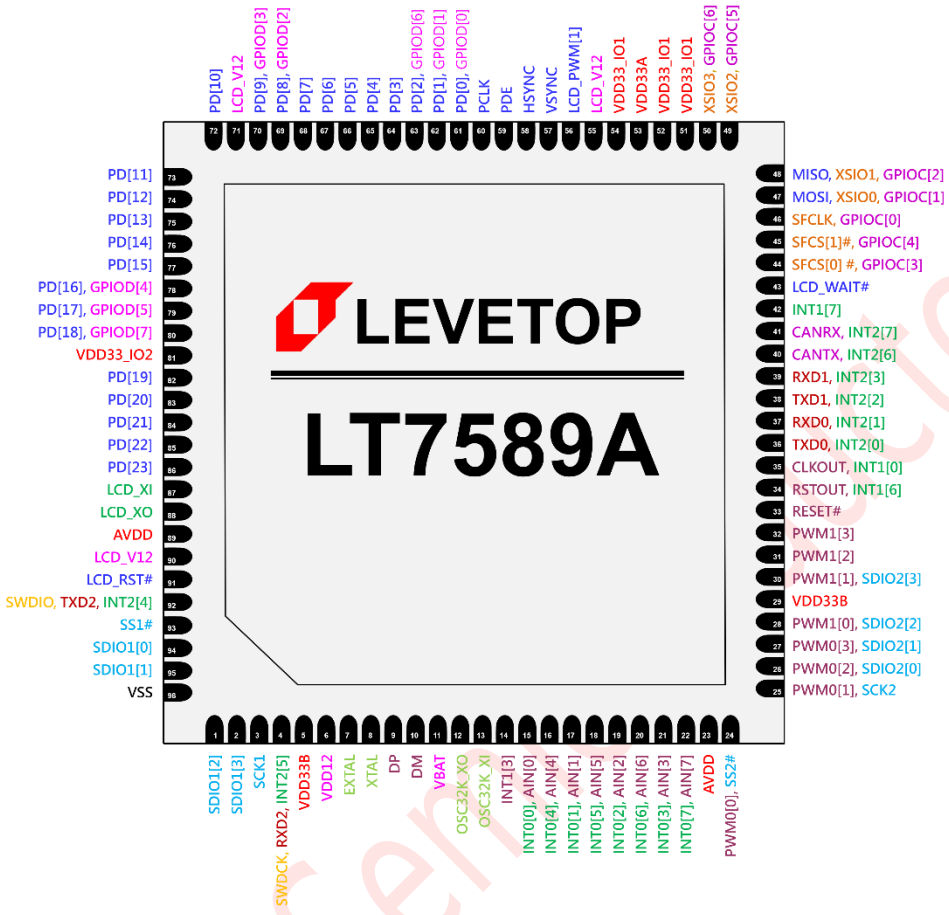


Figure 2-1: LT7589A Pin Assignment (QFN-96Pin)

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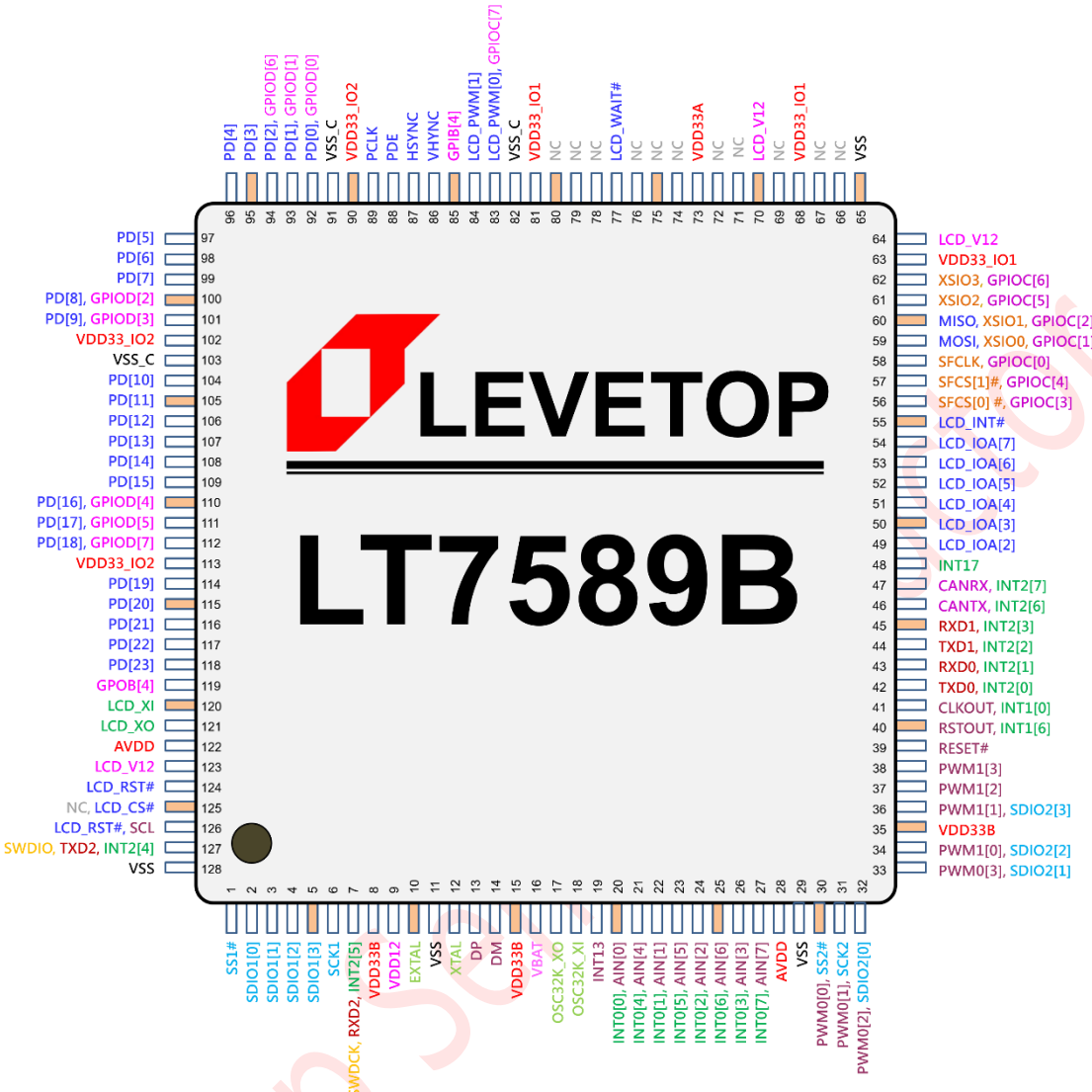


Figure 2-2: LT7589B Pin Assignment (LQFP-128Pin)

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2.2. Pin Description

2.2.1. SCI (Uart) Signals

Table 2-1: SCI (Uart) Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
37	43	RXD0	I	**Serial Communication (Uart) #0 Receives Data Input** This signal is used for SCI #0 receiver data input and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[1].
36	42	TXD0	O	**Serial communication (Uart) #0 Transmission Data Output** This signal is used for SCI #0 transmitter data output and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[0].
39	45	RXD1	I	**Serial Communication (Uart) #1 Receives Data Input** This signal is used for SCI #1 receiver data input and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[3].
38	44	TXD1	O	**Serial communication (Uart) #1 Transmission Data Output** This signal is used for SCI #1 transmitter data output and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[2].
4	7	RXD2	I	**Serial Communication (Uart) #2 Receives Data Input** This signal is used for SCI #2 receiver data input and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[5].
92	127	TXD2	O	**Serial communication (Uart) #2 Transmission Data Output** This signal is used for SCI #2 transmitter data output and can be used to connect external SCI interface components or modules. It can also be used as a regular GPIO or interrupt input interface INT2[4].

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2.2.2. LCD Panel Signals

Table 2-2: LCD Panel Signals

<table>
<tr><th>Pin #
LT7589A</th><th>Pin #
LT7589B</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>86~82,
80~72,
70~61</td><td>118~114,
112~104,
101~92</td><td>PD[23:19],
PD[18:10],
PD[9:0]</td><td>O</td><td>LCD Panel Data Bus
TFT LCD data bus output for source driver. User can connect to corresponding RGB bus for different settings.
<table><tr><th rowspan="2">Pin Name</th><th colspan="2">TFT-LCD Interface</th></tr><tr><th>16bits</th><th>24bits</th></tr><tr><td>PD[0]</td><td>GPIOD[0]</td><td>B0</td></tr><tr><td>PD[1]</td><td>GPIOD[1]</td><td>B1</td></tr><tr><td>PD[2]</td><td>GPIOD[6]</td><td>B2</td></tr><tr><td>PD[3]</td><td>B0</td><td>B3</td></tr><tr><td>PD[4]</td><td>B1</td><td>B4</td></tr><tr><td>PD[5]</td><td>B2</td><td>B5</td></tr><tr><td>PD[6]</td><td>B3</td><td>B6</td></tr><tr><td>PD[7]</td><td>B4</td><td>B7</td></tr><tr><td>PD[8]</td><td>GPIOD[2]</td><td>G0</td></tr><tr><td>PD[9]</td><td>GPIOD[3]</td><td>G1</td></tr><tr><td>PD[10]</td><td>G0</td><td>G2</td></tr><tr><td>PD[11]</td><td>G1</td><td>G3</td></tr><tr><td>PD[12]</td><td>G2</td><td>G4</td></tr><tr><td>PD[13]</td><td>G3</td><td>G5</td></tr><tr><td>PD[14]</td><td>G4</td><td>G6</td></tr><tr><td>PD[15]</td><td>G5</td><td>G7</td></tr><tr><td>PD[16]</td><td>GPIOD[4]</td><td>R0</td></tr><tr><td>PD[17]</td><td>GPIOD[5]</td><td>R1</td></tr><tr><td>PD[18]</td><td>GPIOD[7]</td><td>R2</td></tr><tr><td>PD[19]</td><td>R0</td><td>R3</td></tr><tr><td>PD[20]</td><td>R1</td><td>R4</td></tr><tr><td>PD[21]</td><td>R2</td><td>R5</td></tr><tr><td>PD[22]</td><td>R3</td><td>R6</td></tr><tr><td>PD[23]</td><td>R4</td><td>R7</td></tr></table>When the LCD is set to 16/18bpp function mode, some PDs can be defined as GPIO pins.</td></tr>
<tr><td>60</td><td>89</td><td>PCLK</td><td>O</td><td>Pixel Clock
Generic TFT interface signal for panel scan clock. It derives from internal PLL.</td></tr>
</table>

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
57	86	VSYNC	O	**VSYNC Pulse Signal** Generic TFT interface signal for vertical synchronous pulse.
58	87	HSYNC	O	**HSYNC Pulse Signal** Generic TFT interface signal for horizontal synchronous pulse.
59	88	PDE	O	**Data Enable Signal** Generic TFT interface signal for data valid or data enable.

2.2.3. QSPI Signals

Table 2-3: QSPI Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
3	6	SCK1	O	**QSPI #1 Serial Clock Signal** This signal is the clock signal output of the first group SPI and can be used to connect components or modules of external SPI interfaces.
93	1	SS1#	O	**QSPI #1 Chip Selection Signal** This signal is the chip selection output of the first group SPI.
94	2	SDIO1[0]	IO	**Data Output/Input Signal of QSPI #1** This signal is the output/input signal of the first group QSPI data 0.
95	3	SDIO1[1]	IO	**Data Output/Input Signal of QSPI #1** This signal is the output/input signal of the first group QSPI data 1.
1	4	SDIO1[2]	IO	**Data Output/Input Signal of QSPI #1** This signal is the output/input signal of the first group QSPI data 2.
2	5	SDIO1[3]	IO	**Data Output/Input Signal of QSPI #1** This signal is the output/input signal of the first group QSPI data 3.
25	31	SCK2 PWM0[1]	O	**QSPI #2 Serial Clock Signal** This signal is the clock signal output of the second group SPI and can be used to connect components or modules of external SPI interfaces. This pin shares with pin PWM0[1].
24	30	SS2# PWM0[0]	O	**QSPI #2 Chip Selection Signal** This signal is the chip selection output of the second group SPI. This pin shares with pin PWM0[0].

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
26	32	SDIO2[0] PWM0[2]	IO	**Data Output/Input Signal of QSPI #2** This signal is the output/input signal of the second group QSPI data 0. This pin shares with pin PWM0[2].
27	33	SDIO2[1] PWM0[3]	IO	**Data Output/Input Signal of QSPI #2** This signal is the output/input signal of the second group QSPI data 1. This pin shares with pin PWM0[3].
28	34	SDIO2[2] PWM1[0]	IO	**Data Output/Input Signal of QSPI #2** This signal is the output/input signal of the second group QSPI data 2. This pin shares with pin PWM1[0].
30	36	SDIO2[3] PWM1[1]	IO	**Data Output/Input Signal of QSPI #2** This signal is the output/input signal of the second group QSPI data 3. This pin shares with pin PWM1[1].

2.2.4. External Flash Signals

Table 2-4: External Flash Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
45	57	SFCS[1]# GPIOC[4]	IO	**External Serial Flash #1 Chip Selection Signal** This signal is controlled by the LCD controller inside LT7589. If the serial QSPI function is disabled, this pin can be set to GPOC[4], which defaults to input function. **Note:** Under the serial panel function framework of Levetop Semiconductor, only SFCS[1]# is allowed to be used as the chip selection signal for external QSPI Flash, and SFCS[0]# cannot be used.
44	56	SFCS[0]# GPIOC[3]	IO	**External Serial Flash #0 Chip Selection Signal** This signal is controlled by the LCD controller inside LT7589. If the serial QSPI function is disabled, this pin can be set to GPOC[3], which defaults to input function. **Note:** Under the serial panel function framework of Levetop Semiconductor, this signal cannot be used as the chip selection signal for external QSPI Flash, and SFCS[1]# must be used. SFCS[0]# can only be used when the customer develops it with own code.

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
46	58	SFCLK GPIOC[0]	IO	**External Serial Flash Clock Signal** This pin is a serial clock signal output, controlled by the LCD controller inside LT7589, and connected to external Serial Flash or QSPI components. If the serial QSPI function is disabled, this pin can be set to GPOC[0] and default to input function.
47	59	XSIO0 GPIOC[1]	IO	**QSPI Data Input/Output Signal 0** This signal is controlled by the LCD controller inside LT7589, and this data line is connected to an external Serial Flash or QSPI component. If the serial SPI function is disabled, this pin can be set to GPOC[1] and default to input function.
48	60	XSIO1 GPIOC[2]	IO	**QSPI Data Input/Output Signal 1** This signal is controlled by the LCD controller inside LT7589, and this data line is connected to an external Serial Flash or QSPI component. If the serial SPI function is disabled, this pin can be set to GPOC[2] and default to input function.
49	61	XSIO2 GPIOC[5]	IO	**QSPI Data Input/Output Signal 2** This signal is controlled by the LCD controller inside LT7589, and this data line is connected to an external Serial Flash or QSPI component. If the serial SPI function is disabled, this pin can be set to GPOC[5] and default to input function.
50	62	XSIO3 GPIOC[6]	IO	**QSPI Data Input/Output Signal 3** This signal is controlled by the LCD controller inside LT7589, and this data line is connected to an external Serial Flash or QSPI component. If the serial SPI function is disabled, this pin can be set to GPOC[6] and default to input function.

2.2.5. PWM Signals

Table 2-5: PWM Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
--	83	LCD_PWM[0] GPIOC[7]	IO	**LCD PWM#0 Output Signal** This signal is controlled by the register of the LCD controller inside LT7589, and is a programmable PWM output signal that can be used to control the backlight or other components of the TFT LCD screen. The output mode of LCD_PWM can be set through the registers of the LCD controller. This pin shares with pin GPOC[7].

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
56	84	LCD_PWM[1]	IO	**LCD PWM#1 Output Signal** This signal is controlled by the register of the LCD controller inside LT7589, and is a programmable PWM output signal that can be used to control the backlight or other components of the TFT LCD screen. The output mode of LCD_PWM [1] can be set through the registers of the LCD controller.
24	30	PWM0[0] SS2#	IO	**The PWM0[0] Output Signal Controlled by MCU** Can be used as PWM output or GPIO, set by internal MCU registers. This pin shares with pin SS2#.
25	31	PWM0[1] SCK2	IO	**The PWM0[1] Output Signal Controlled by MCU** Can be used as PWM output or GPIO, set by internal MCU registers. This pin shares with pin SCK2.
26	32	PWM0[2] SDIO2[0]	IO	**The PWM0[2] Output Signal Controlled by MCU** Can be used as PWM output or GPIO, set by internal MCU registers. This pin shares with pin SDIO2[0].
27	33	PWM0[3] SDIO2[1]	IO	**The PWM0[3] Output Signal Controlled by MCU** Can be used as PWM output or GPIO, set by internal MCU registers. This pin shares with pin SDIO2[1].
28	34	PWM1[0] SDIO2[2]	IO	**The PWM1[0] Output Signal Controlled by MCU** Can be used as PWM output or GPIO, set by internal MCU registers. This pin shares with pin SDIO2[2].
30	36	PWM1[1] SDIO2[3]	IO	**The PWM1[1] Output Signal Controlled by MCU** Can be used as PWM output or GPIO, set by internal MCU registers. This pin shares with pin SDIO2[3].
31	37	PWM1[2]	IO	**The PWM1[2] Output Signal Controlled by MCU** Can be used as PWM output or GPIO, set by internal MCU registers.
32	38	PWM1[3]	IO	**The PWM1[3] Output Signal Controlled by MCU** Can be used as PWM output or GPIO, set by internal MCU registers.

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2.2.6. USB Signals

Table 2-6: USB Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
9	13	DP	IO	**USB Data Port (Positive)** This is the signal of USB data terminal DP.
10	14	DM	IO	**USB Data Port (Negative)** This is the signal of USB data terminal DM.

2.2.7. GPIO and Interrupt Signals

Table 2-7: GPIO and Interrupt Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
15	20	INT0[0] AIN[0]	I	**Interrupt INT0[0] Signal** Can be used as an interrupt input or as an analog signal input.
17	22	INT0[1] AIN[1]	I	**Interrupt INT0[1] Signal** Can be used as an interrupt input or as an analog signal input.
19	24	INT0[2] AIN[2]	I	**Interrupt INT0[2] Signal** Can be used as an interrupt input or as an analog signal input.
21	26	INT0[3] AIN[3]	I	**Interrupt INT0[3] Signal** Can be used as an interrupt input or as an analog signal input.
16	21	INT0[4] AIN[4]	I	**Interrupt INT0[4] Signal** Can be used as an interrupt input or as an analog signal input.
18	23	INT0[5] AIN[5]	I	**Interrupt INT0[5] Signal** Can be used as an interrupt input or as an analog signal input.
20	25	INT0[6] AIN[6]	I	**Interrupt INT0[6] Signal** Can be used as an interrupt input or as an analog signal input.
22	27	INT0[7] AIN[7]	I	**Interrupt INT0[7] Signal** Can be used as an interrupt input or as an analog signal input.
36	42	INT2[0] TXD0	I	**Interrupt INT2[0] Signal** Can be used as an interrupt input. This pin shares with pin TXD0.
37	43	INT2[1] RXD0	IO	**Interrupt INT2[1] Signal** Can be used as an interrupt input. This pin shares with pin RXD0.
38	44	INT2[2] TXD1	I	**Interrupt INT2[2] Signal** Can be used as an interrupt input. This pin shares with pin TXD1.

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
39	45	INT2[3] RXD1	IO	**Interrupt INT2[3] Signal** Can be used as an interrupt input. This pin shares with pin RXD1.
92	127	INT2[4] TXD2	I	**Interrupt INT2[4] Signal** Can be used as an interrupt input. This pin shares with pin TXD2.
4	7	INT2[5] RXD2	IO	**Interrupt INT2[5] Signal** Can be used as an interrupt input. This pin shares with pin RXD2.
40	46	INT2[6] CANTX	I	**Interrupt INT2[6] Signal** Can be used as an interrupt input. This pin shares with pin CANTX.
41	47	INT2[7] CANRX	IO	**Interrupt INT2[7] Signal** Can be used as an interrupt input. This pin shares with pin CANRX.
35	41	INT1[0] CLKOUT	IO	**Interrupt INT1[0] Signal** Can be used as an interrupt input. This pin shares with pin CLKOUT.
14	19	INT1[3]	IO	**Interrupt INT1[3] Signal** Can be used as an interrupt input.
34	40	INT1[6] RSTOUT	IO	**Interrupt INT1[6] Signal** Can be used as an interrupt input. This pin shares with pin RSTOUT.
42	48	INT1[7]	IO	**Interrupt INT1[7] Signal** Can be used as an interrupt input.
--	55	LCD_INT#	O	**LCD Interrupt Output Signal** When the interrupt condition set by the LCD controller occurs, this pin becomes low and is used to generate an interrupt output to inform the MCU.
--, 50, 49, 45, 44, 48, 47, 46	83, 62, 61, 57, 56, 60, 59, 58	GPIOC[7] GPIOC[6:0]	IO	**GPIO Output/Input Signals of LCD Controller** These signals are controlled by the register of the LCD controller inside LT7589, and the output data of GPOC[7] shares pins with LCD_PWM[0]. GPOC [6:0] shares pins with {XSIO3, XSIO2, SFC[1] #, SFC[0] #, XSIO1, XSIO0, SFCLK} and can only be used when the functions of LCD_PWM and SPI Master are disabled. The output mode of these pins can be set through the registers of the TFT LCD controller.

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
80, 63, 79, 78, 70, 69, 62, 61	112, 94, 111, 110, 101, 100, 93, 92	GPIOD[7:0]	IO	**GPIO Output/Input Signals of LCD Controller** These signals are controlled by the register of the LCD controller inside LT7589, and the output data of GPOD [7:0] shares pins with {PD[18], PD[2], PD[17], PD[16], PD[9], PD[8], PD[1], PD[0]}. GPOD[7:0] can only be used when the LCD panel data bus is set to 16 bits. The output mode of these pins can be set through the registers of the TFT LCD controller.
--	54~49	LCD_IOA[7:2]	IO	**GPIO Output/Input Signals of LCD Controller** The output/input modes of these pins can be set through the registers of the TFT LCD controller.

2.2.8. ADC Input Signals

Table 2-8: ADC Input Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
22, 20, 18, 16, 21, 19, 17, 15	27, 25, 23, 21, 26, 24, 22, 20	AIN[7:0] INT0[7:0]	IO	**Analog Input Signals** These analog signals are used as ADC analog input channels. When not configured as analog inputs, these signals can also be used for INT0[7:0].

2.2.9. Miscellaneous Signals

Table 2-9: Miscellaneous Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
43	77	LCD_WAIT#	O	**Waiting for Output Signal** When the internal MCU performs read and write control on the LCD control circuit, if it is in a busy state, WAIT # will be set to a low potential to inform the MCU to enter the waiting cycle.
--	125	LCD_CS# NC	I	**LCD Control Circuit Chip Selection Signal** LCD_CS# = 0, Represents the command or data read/write cycle of the internal MCU to the LCD control circuit. Note: This pin has already been internally connected to the EBI-CS # of the MCU and must be kept in NC.
91	124	LCD_RST#	I	**Reset Input Signal for LCD Control Circuit** When RST #=0 and maintains a length greater than 32 clock cycles, LT7586 will generate a reset action.
--	126	SCL LCD_RST#	IO	**I2C Clock Signal** This signal is used as the clock signal for I2C of MCU or GPIO. Note: This pin should be connected to the LCD_RST# of Pin-124 to control whether the LCD circuit performs a reset action.

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
4	7	SWDCK RXD2, INT2[5]	I	**Flash Programming Clock Signal** This input signal is the clock signal used for programming internal flash memory. This pin is also connected to RXD2 and INT2[5], it's a shared pin.
92	127	SWDIO TXD2, INT2[4]	I	**Flash Programming Data Signal** This input signal is used as a data signal for programming internal flash memory. This pin is also connected to TXD2 and INT2[4], it's a shared pin.
35	41	CLKOUT INT1[0]	O	**System Clock Signal Output** This output signal reflects the internal system clock. When not configured as a clock output, this signal can also be used for INT1[0].
34	40	RSTOUT INT1[6]	O	**MCU Reset Output Signal** This output signal indicates that the internal reset controller is resetting the chip. 0 = The chip is in a reset state 1 = chip not reset state When not configured as a reset output, this signal can also be used for INT1[6].
33	39	RESET#	I	**MCU Reset Input Signal** When RESET#=0, a reset action will be performed on the internal MCU.

2.2.10. Power and Clock Signals

Table 2-10: Power and Clock Signals

Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
87	120	LCD_XI	I	**LCD Crystal/Clock Signal Input** This pin is connected to an external crystal oscillator and serves as the input signal for the crystal oscillator circuit of the internal TFT LCD controller. When using an active crystal oscillator or an external clock signal, it can be input through this pin. Typically, this clock signal is connected to pin "XTAL" , and the recommended crystal oscillator frequency (OSC) is 12MHz.
88	121	LCD_XO	O	**LCD Crystal Output** This pin is connected to an external crystal oscillator and outputs a signal to the crystal oscillator circuit of the internal TFT controller.

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
13	18	OSC32K_XI	I	**32.768Khz Crystal Oscillator Input** RTC clock signal, this pin is connected to an external 32.768Khz crystal oscillator.
12	17	OSC32K_XO	O	**32.768Khz Crystal Oscillator Output** RTC clock signal, this pin is connected to an external 32.768Khz crystal oscillator.
8	12	XTAL	I	**USB Clock Signal** This pin is connected to an external 12MHz crystal oscillator.
7	10	EXTAL	O	**USB Clock Signal** This pin is connected to an external 12MHz crystal oscillator.
11	16	VBAT	PWR	**3.3V~3.6V Battery Power Input (RTC)** An external filtering capacitor must be connected to ensure stable power supply.
53	73	VDD33A	PWR	**3.3V Power Input (LCD)** Near the pin end, an external 10uF and a 0.1uF filtering capacitor must be connected to ground. Note: This power input should be powered independently and should not be directly connected to VDD33_iO or AVDD.
5, 29	8, 15, 35	VDD33B	PWR	**3.3V Power Input (MCU)** This pin requires an external 1uF and 0.1uF filtering capacitor to be connected to ground and ensure stable power supply.
51, 52, 54	63, 68, 81	VDD33_IO1	PWR	**3.3V Power Input (I/O)** This pin requires an external 2.2uF and 0.1uF filtering capacitor to be connected to ground and ensure stable power supply.
81	90, 102, 113	VDD33_IO2	PWR	**3.3V Power Input (I/O)** These pins must be connected to an external 2.2uF and 0.1uF filtering capacitor to ground, and separated from VDD33_IO1 to ensure stable power supply Please refer to the application circuit in Chapter 9.
23, 89	28, 22	AVDD	PWR	**Power Input of Internal Analog Circuit** Provide 3.3V voltage, and a 1uF and a 0.1uF filtering capacitor must be externally connected to the ground near the pin end.
6	9	VDD12	PWR	**1.2V Core Power Output (MCU)** Near the pin end, an external 1uF and a 0.1uF filtering capacitor must be connected to ground.

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Pin # LT7589A	Pin # LT7589B	Pin Name	I/O	Description
55, 71, 90	64, 70, 123	LCD_V12	PWR	**1.2V Core Power Output (LCD)** Just connect an external 0.01uF filtering capacitor to ground near the pin end. Note: The external capacitor should not exceed 0.01uF and should not be connected to VDD12.
96	11, 29, 65, 28	VSS	PWR	**GND Ground**
--	82, 91, 103	VSS_C	PWR	**Core GND Ground**
0	--	Thermal Pad	-	**Heat Dissipation Pad** The heat dissipation pads on the back of the LT7589B package must be directly grounded. Note: In order to achieve better soldering results, it is recommended to refer to the instructions in Figure 8-3 when PCB Layout.

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2.3. GPIO Resources of Different TFT Panels

Table 2-11: LT7589A GPIO Resources

Chip / Functions	LT7589A (QFN-96)	
TFT Panel Data	RGB 565 I/F	RGB 888 I/F
Resolution(Max.)	1280x800 (Serial Protocol Mode)	1280x800 (Serial Protocol Mode)
Flash	2MB	2MB
SRAM	256KB+512KB	256KB+512KB
Display RAM	16MB	16MB
USB 2.0	V (DP/DM)	V (DP/DM)
RTC	V	V
SCI Communication Port	V (RXD1, TXD1)	V (RXD1, TXD1)
Ext. SPI Flash	V (758_SF)	V (758_SF)
Back-Light Control	V (758_PWM1)	V (758_PWM1)
SWD Programming Port	V (SWD)	V (SWD)

TP Type / IO Port	xTP (1)	CTP	RTP (2)	xTP	CTP	RTP
Total Number of IO Ports	38	34	33	30	26	25
IO Port Type Description	GPIO (2), GINT, PWM, SCI, QSPI, ADCIN	GPIO (2), GINT, PWM, SCI, QSPI, ADCIN	GPIO (2), GINT, PWM, SCI, QSPI, ADCIN	GINT, PWM, SCI, QSPI, ADCIN	GINT, PWM, SCI, QSPI, ADCIN	GINT, PWM, SCI, QSPI, ADCIN

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Table 2-12: LT7589B GPIO Resources

Functions \ Chip	LT7589B (LQFP-128)	
TFT Panel Data	RGB 565 I/F	RGB 888 I/F
Resolution(Max.)	1280x800 (Serial Protocol Mode)	1280x800 (Serial Protocol Mode)
Flash	2MB	2MB
SRAM	256KB+512KB	256KB+512KB
Display RAM	16MB	16MB
USB 2.0	V (DP/DM)	V (DP/DM)
RTC	V	V
SCI Communication Port	V (RXD1, TXD1)	V (RXD1, TXD1)
Ext. SPI Flash	V (758_SF)	V (758_SF)
Back-Light Control	V (758_PWM1)	V (758_PWM1)
SWD Programming Port	V (SWD)	V (SWD)

IO Port \ TP Type	xTP (1)	CTP	RTP (2)	xTP	CTP	RTP
Total Number of IO Ports	46	42	41	38	34	33
IO Port Type Description	GPIO (2), GINT, PWM, SCI, QSPI, ADCIN	GPIO (2), GINT, PWM, SCI, QSPI, ADCIN	GPIO (2), GINT, PWM, SCI, QSPI, ADCIN	GPIO, GINT, PWM, SCI, QSPI, ADCIN	GPIO, GINT, PWM, SCI, QSPI, ADCIN	GPIO, GINT, PWM, SCI, QSPI, ADCIN

Notes:

(1) XTP means without TP

(2) Add 8 GPIO

(3) RTP needs to add an RTP control chip (such as TSC2046)

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3. Function Description

The LT7589 integrates a high-performance 32-bit MCU and a TFT LCD graphic display controller (hereinafter referred to as the TFT LCD controller). The main architecture of this MCU is the same as that of the LT32U05 from Levetop Semiconductor, with 2Mbytes of Flash program space and 768Kbytes of SRAM. Its functions can be directly referred to in the LT7589 MCU core specification or application manual. Therefore, the functional part of the 32-bit MCU will not be described in detail in this specification. In addition, the TFT LCD graphics accelerator adopts the LT7586 hardware architecture of Levetop Semiconductor, with 128Mbytes of display memory and JPG decoder. Its connection with the 32-bit MCU is shown in the following figure:

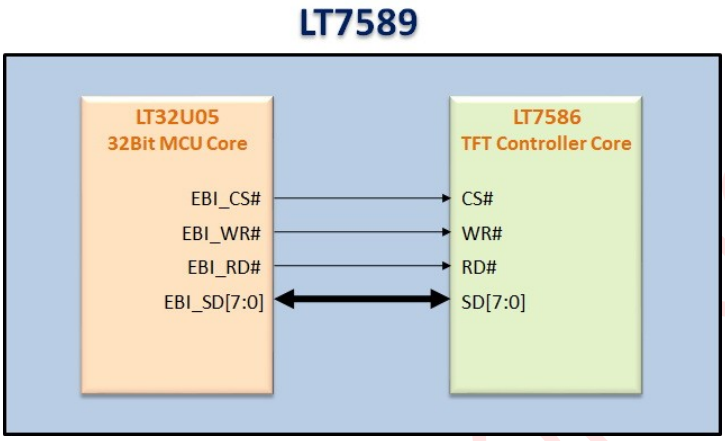


Figure 3-1: Communication Mode between LT7589 Internal MCU and TFT Graphics Accelerator

3.1. Serial Uart Interface

When using LT7589 as a Serial Uart TFT controller, its communication mode with the Host control MCU is through the Uart interface. LT7589 has three sets of SCI (Uart) serial ports, and by default, the second set of TXD1 and RXD1 is used to communicate with the main control MCU. As for the development of the internal MCU program of LT7589, please refer to the LT7589 application manual. Levetop Semiconductor also provides a complete development environment or programming tool.

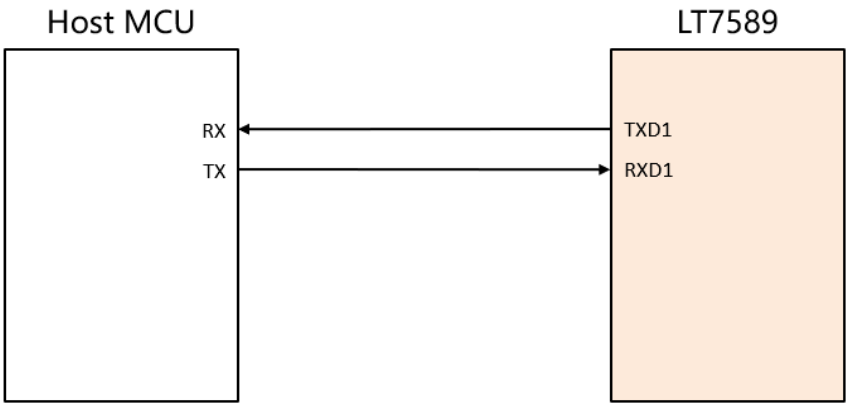


Figure 3-2: Communication Mode with the Host MCU

When developing as a serial Uart TFT Controller, the internal MCU program of LT7589 will provide a serial protocol program. Users can use the UI_Editor software provided by Levetop Semiconductor to import the already designed UI structure flow such as images and animations, and complete the development of TFT display. Basically, there is no need to modify the internal MCU program of LT7589, nor do they need to understand the internal registers and control methods of LT7589. The host control MCU program only needs to send the instruction format of the serial protocol according to the product application, and receive and interpret the feedback information sent by LT7589. Therefore, it saves a lot of time in TFT panel display

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development work.

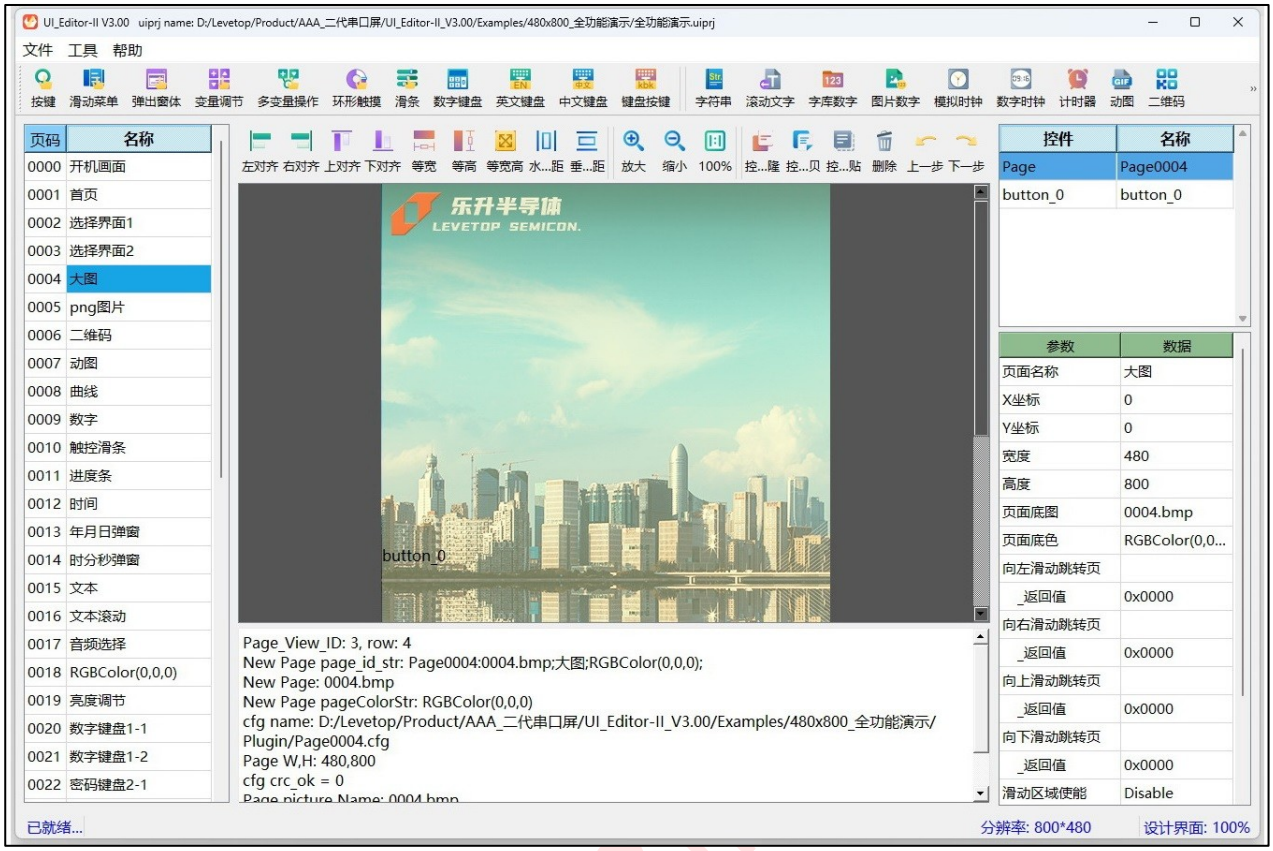


Figure 3-3: The Main Screen of UI_Editor Tool

Note: When developing the LT7589 serial Uart TFT Controller, the internal 2Mbytes Flash is used to store the boot program and serial protocol program. During the sample development stage, the samples provided by Levetop Semiconductor will include the boot program, making it convenient for users to update the serial protocol program and develop or modify their own code. During the mass production stage, the chip provided does not include any program (Flash is blank), and users must burn it themselves during production. For code updates and programming, please refer to the LT7589 programming manual.

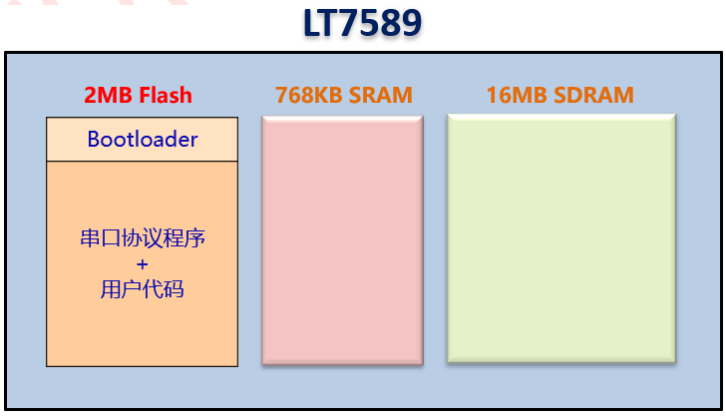


Figure 3-4: LT7589 Internal Memory

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3.2. Serial TFT Panel Protocol Table

LT7589 supports the development of the third-generation UI_Editor-III serial TFT panel software by Levetop Semiconductor. The UI_Editor-III adopts variable control mode, and serial communication and instructions are shown in the following table:

Table 3-1: Serial Communication and Instruction Differences of UI-Editor-III

Mode	UI_Editor-III
Serial Communication	Composed of "frame header + length + read/write instruction code + variable data + CRC", the frame header can be modified and supports Modbus, I2C.
Instructions	The serial instruction only performs variable read and write operations, and the serial port does not correspond one-to-one with the function. The number of individual functions is not limited.

The following table shows the serial TFT panel protocols supported by LT7589 in UI_Editor-III mode:

Table 3-2: UI_Editor-III's Command Format for Serial Communication

Instruction Mode	Head (2 Bytes)	Length (1Byte)	Instruction Code (1Byte)	Variable Address (2 Bytes)	Data1 (2*n Bytes)	Data2	CRC (2 Bytes)
Write Variable Instruction (Sending Data Through Serial Port)	0x5AA5	0xXX	0x10 (Write Command)	0x0000~0x5FFF	Write Data (2*n Bytes)	NULL	0xXXXX
Read Variable Instruction	0x5AA5	0xXX	0x03 (Read Command)	0x0000~0x5FFF	Number of Word read out (2 Bytes)	NULL	0xXXXX
Return Instruction Format	0x5AA5	0xXX	0x03 (Read Instruction)	0x0000~0x5FFF	Number of Word read out (2 Bytes)	Data (2*n Bytes)	0xXXXX
Touch Feedback Command	0x5AA5	0xXX	0x41	**Variable Address** (Register Address)	Returned KeyValue (2 Bytes)	NULL	0xXXXX

For the UI_Editor-III communication mode, please refer to the UI_Editor-III's user manual.

3.3. Program Code Develop

Due to its high capacity of Flash and SRAM, LT7589 can also be used as a main control MCU with a TFT controller. The main control and TFT display functions can be completed by one LT7589, or when customers need to use LT7589 and require internal MCU resources or make some program modifications for secondary development, they need to refer to the internal 32-bit MCU specifications in Chapter 4 or contact the FAE of Levetop Semiconductor.

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3.4. The Application of Chip's Interface

The previous chapter mentioned that the communication mode of the main control MCU is through the Uart(0) interface, while other interfaces will be described in this chapter.

3.4.1. Interface of TFT LCD Panel

LT7589 is connected to a standard TFT LCD RGB panel using data lines and four control signals: HSYNC, VSYNC, PDE, PCLK (as shown in the figure below). If RGB: 888 is used, 24 data lines are required. If RGB: 565 is used, 16 data lines are required. Unused data lines can be used as IO ports, as shown in Table 3-3 below. The actual application schematic can refer to Chapter 29.

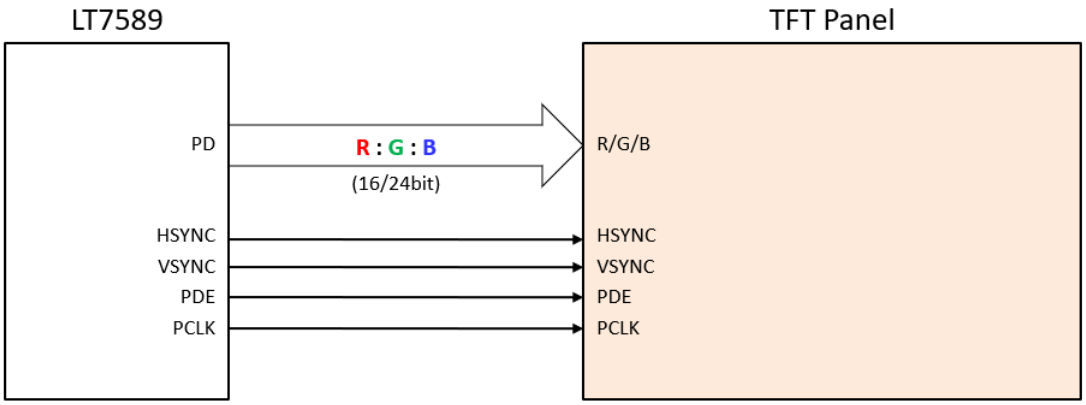


Figure 3-5: Connection Between LT7589 and TFT LCD Panel

Table 3-3: RGB Data and Color Depth

RGB Signals	LCD Data Bus	Color Depth
R:G:B = 8:8:8	PD[23~0]	16.7M
R:G:B = 5:6:5	PD[23~19], PD[15~10], PD[7~3]	65K

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3.4.2. SSI (Synchronous Serial Interface)

3.4.2.1. SSI interface on TFT LCD Controller

As a serial Uart TFT Controller, the SSI interface of the TFT LCD controller of LT7589 is specifically connected to the external QSPI Flash. Most of the LCD display materials are stored in the external Flash of this interface. LT7589 adopts high-speed DMA transfer mode, reads UI material data through the fast QSPI interface, writes it into the internal SDRAM display, and then sends the SDRAM data to the TFT LCD panel through the internal scanning circuit. The LT7589 TFT controller can simultaneously connect 2 external Flash devices and supports NOR or NAND Type Flash. If NAND Flash is used, the LT7589 also supports bad block handling for Flash.

Under the framework of using the serial panel function of Levetop Semiconductor, only SFCS[1]# is allowed to be used as the chip selection signal for external QSPI Flash, while SFCS[0]# is only reserved for customers to use own code to development, as shown in the following figure.

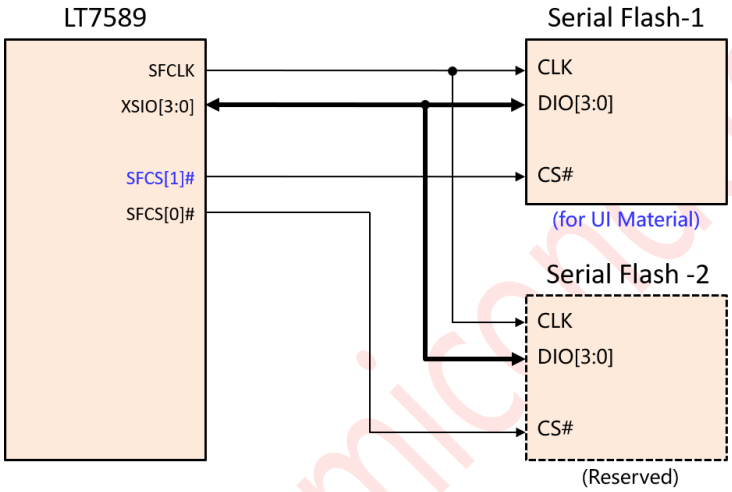


Figure 3-6: Schematic Diagram of the Connection Between LT7589 and QSPI Flash

3.4.2.2. SSI interface on MCU End

In addition to the QSPI interface provided by the TFT LCD controller, LT7589 also offers two completely independent SSI synchronous serial interfaces on the MCU side, which can be connected to SPI Flash or other SPI interface components, as shown in the following figure. The QSPI interface of Group 2 is shared with some pins of PWM0 and PWM1, please refer to Sections 2.2.3 and 2.2.5. If the customer wants to develop and control these SSI signals for the second time, please refer to Chapter 21 for instructions. At the same time, these SSI signals can also be set for GPIO use. Please refer to Chapter 6's Chip Configuration Module (CCM) instructions.

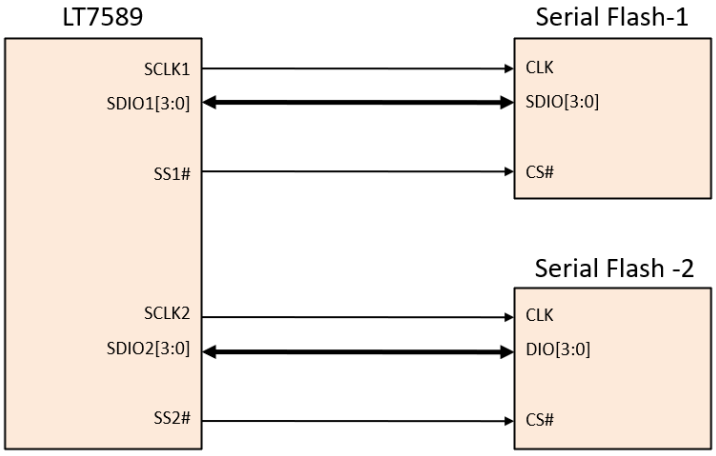


Figure 3-7: Schematic Diagram of QSPI Flash Connection to LT7589 MCU End

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3.4.3. SCI (Serial Communication Interface)

LT7589 provides three sets of SCI serial ports. As mentioned earlier, the second set TXD1 and RXD1 are used by default to communicate with the main control MCU, while the other 2 sets can be used to connect Bluetooth modules, WiFi modules, or other serial components, as shown in the following figure. The TXD0, RXD0, TXD2, and RXD2 interfaces can also be set as INT interrupt inputs or GPIO ports through registers. Please refer to the relevant pin signal descriptions in sections 2.2.1 and 2.2.7. If users want to develop and control these SCI input signals again, please refer to Chapter 20 for instructions.

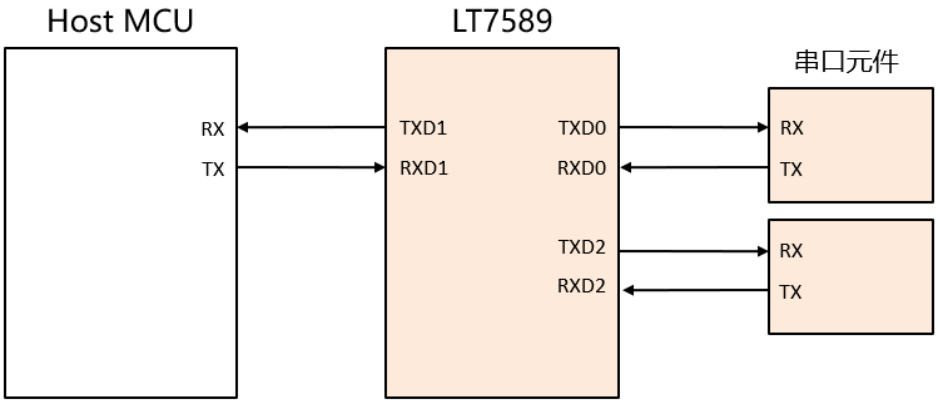


Figure 3-8: LT7589 Provides Three Sets Of SCI Serial Ports

3.4.4. ADC Analog Input

LT7589 provides eight analog input interfaces, which can also be individually converted into interrupt input interfaces through register settings, as shown in the following figure. The AIN interface is shared with the INT0 pin, please refer to section 2.2.8. If users want to develop and control these ADC input signals again, please refer to Chapter 25 for instructions. The LT7589 also comes with a comparator internally, which can be used through the ADC analog input interface. Please refer to Chapter 23 for details.

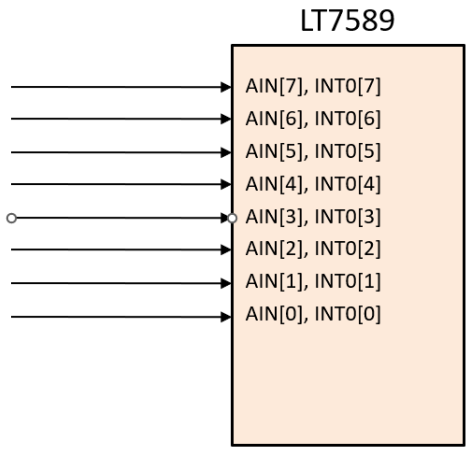


Figure 3-9: LT7589 Provides Eight Analog Input

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3.4.5. GPIO and Interrupt Signals

3.4.5.1. The GPIO and Interrupt Input of MCU End

In the previous section 2.2.7, it was mentioned that LT7589 has three sets of interrupt signals at the MCU end: INT0, INT1, INT2, Among them, INT0 shares with AIN, and INT2 shares with SCI and Canbus serial port signals, as shown in the following figure. The MCU of LT7589 has an embedded interrupt controller (EIC). If users want to use these interrupt input signals through secondary development, please refer to the instructions in Chapter 6 Chip Configuration Module (CCM) and Chapter 7 Embedded Interrupt Controller (EIC).

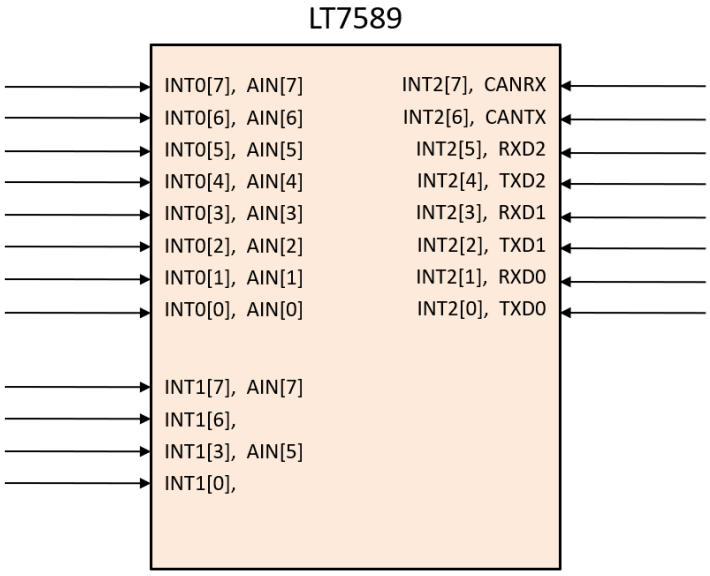


Figure 3-10: The GPIO and Interrupt Input of MCU End

3.4.5.2. The GPIO of TFT LCD Controller

There are also some GPIO interfaces provided within the TFT LCD controller, which can serve as extensions of the MCU interface. Among them, the GPIO[7:0] interface shares pins with the LCD screen data line (as shown in the table below). The LT7589B also has an additional set of LCD_IOA[7:2] interfaces, which are set as outputs or inputs. The TFT LCD controller registers for outputting or reading input data are REG[F5-F6h]. Please refer to Section 26.2 for the GPIO register description of the TFT LCD controller.

Table 3-4: GPIO Signals Shares Pins With Other Control Signals

GPIO Signals Provided by TFT LCD Controller	Share Pins
GPIOD[7:0]	Share with pin - PD[18, 2, 17, 16, 9, 8, 1, 0] , and can only be used when the LCD screen data bus is set to 16 bits. The output mode of these pins can be set through registers.
GPIOC[7]	Share with pin - LCD_PWM[0]
LCD_IOA[7:2]	None (only available for LT7589B)

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3.4.6. PWM Output Signals

3.4.6.1. PWM Outputs of MCU End

LT7589 also provides 2 sets of PWM outputs at the MCU end, each with 4 channels, as shown in the following figure. The interfaces of PWM0[3:0] and PWM1[1:0] are shared with the QSPI pins of Group 2, please refer to Section 2.2.5. If the customer wants to develop and control these PWM output signals again, please refer to Chapter 22 for instructions.

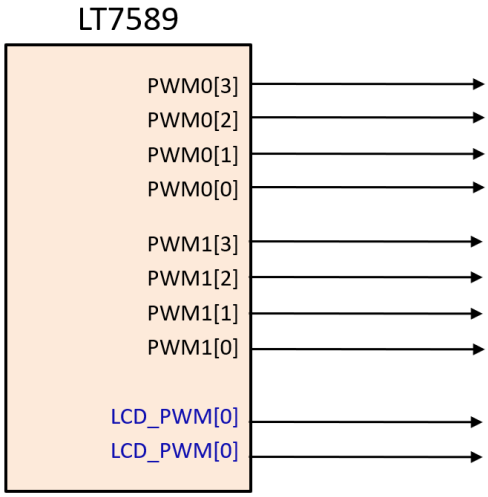


Figure 3-11: PWM Output of LT7589 MCU End

3.4.6.2. PWM Outputs of TFT LCD Controller

LT7589 also provides 2 PWM outputs within the TFT LCD controller: LCD_PWM[0], LCD_PWM[1] (as shown in the above figure). The TFT controller contains two 16 bit counters, Timer-0 and Timer-1, whose actions are related to the output state of LCD_PWM. Taking LCD_PWM [0] as an example, before use, the Timer-0 count register (REG[8Ah-8Bh], TCNTB0) and Timer-0 count comparison register (REG[88h-89h], TCMPB0]) must be set. After starting the PWM function, the Timer-0 counter will first load the value of TCNTB0 and start counting according to the set frequency of the PWM Clock. When the value of the Timer-0 counter is equal to the value of the TCMPB0 register, the PWM will act, that is, if LCD_PWM[0] was originally 0, it will switch to 1, while the Timer-0 counter will continue counting. When Timer-0 continues to count and equals 0, an interrupt will be generated. LCD_PWM[0] returns to its original level of 0 and automatically loads the value of register TCNTB0, representing a complete PWM cycle.

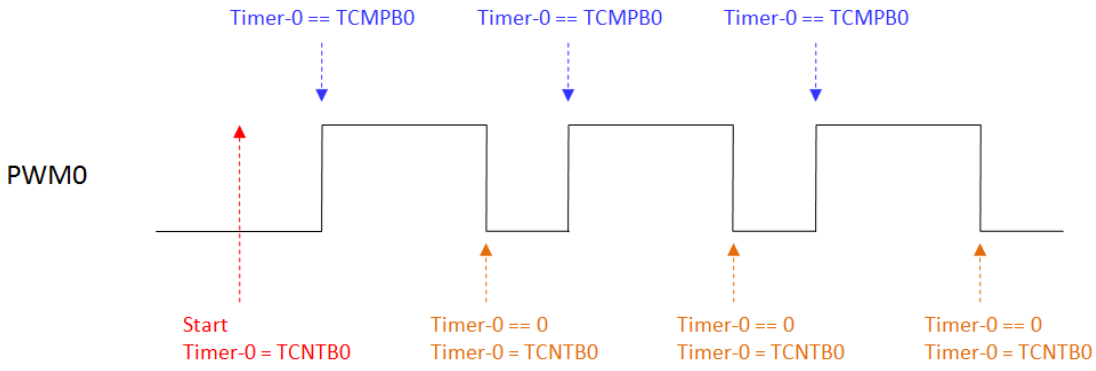


Figure 3-12: LCD_PWM Waveform Diagram

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The above actions can be understood that the Duty of LCD_PWM [0] is determined by the comparison register (REG [88h-89h], TCMPB0]). For example, if you want to generate an approximate DC level voltage through LCD_PWM [0], when LCD_PWM [0] is initially set to 0 and the desired equivalent voltage is high, then the TCMPB0 value needs to be set slightly higher; When LCD_PWM [0] is initially set to 1 and the desired equivalent voltage is high, the TCMPB0 value needs to be set slightly smaller.

It should be noted that the automatic loading function of REG [86h] (PCFGR) must be enabled for Timer-0 to automatically reload the value of register TCNTB0. Therefore, if the MCU changes the value of TCNTB0 or TCMPB0 before Timer-0 equals 0, different Duty dynamic PWM waveforms can be generated.

■ LCD_PWM Timing Source

The timing of the LCD_PWM counter comes from CCLK. The timing fundamental frequencies of Timer-0 and Timer-1 are determined by the register PSCLR (REG [84h]):

Base Clock = CCLK / (Prescaler + 1)

The Clock sent to Timer is then determined by its respective frequency division register (REG[85h]), and each counter's frequency divider can generate four different frequency division options: 1/2, 1/4, and 1/8. For example, if the frequency division register REG[85h] bit[5:4] = 10b, then the Timer-0 count Clock = timing fundamental frequency/4. Please refer to Chapter 26 for the explanation of registers REG[84h] and REG[85h] for TFT LCD controllers.

■ LCD_PWM Output Signal

LCD_PWM can also be set to a fixed high or low level in addition to pulse. If it is LCD_PWM [0], the automatic reload function must be turned off first. The bit 1 of register REG[86h] (PCFGR) is set to 0, and the Timer-0 count is stopped. The bit 0 of register REG[86h] (PCFGR) is set to 0. If Timer-0 < TCMP0, the output value is high, and if Timer-0 > TCMP0, the output value is low (assuming the reverse phase is turned off). The output of LCD_PWM[0] can be inverted by setting the output value through PCFG bit2.

In addition, LCD_PWM[0] and LCD_PWM[1] are shared output pins that can be used for other purposes. Please refer to the description of register REG[85h] (PMUXR) bit[3:0].

Table 3-5: Register REG [85h] Description

Bit	Description
3-2	LCD_PWM [1] Function Control 0xb: LCD_PWM [1] Output system error flag (Scan FIFO pop error or memory access out of range). 10b: LCD_PWM [1] outputs the waveform of PWM counter 1 or the inverted waveform of PWM counter 0 (dead zone enabled). 11b: LCD_PWM [1] outputs the oscillator crystal frequency (OSC)
1-0	LCD_PWM [0] Function Control 0xb: LCD_PWM [0] is GPO-C [7]. 10b: LCD_PWM [0] outputs PWM counter 0. 11b: LCD_PWM [0] outputs the system frequency.

LCD_PWM [0] and LCD_PWM [1] can also be set as complementary outputs. In this case, the output of LCD_PWM [1] follows the setting and control of LCD_PWM [0], but it is the reverse output state of LCD_PWM [0]:

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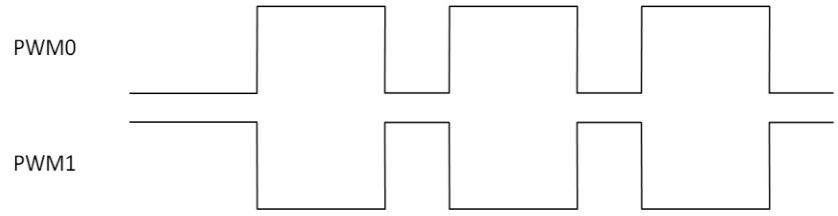


Figure 3-13: LCD_PWM [0] and LCD_PWM [1] Complementary Outputs

In some applications, in order to avoid interference caused by excessive current due to the simultaneous switching of LCD_PWM[0] and LCD_PWM[1], LT7589 provides blind spot timing control, which offsets the simultaneous switching time of LCD_PWM[0] and LCD_PWM[1]. The blind spot spacing is set by the register REG[87h] (DZ_LENGTH):

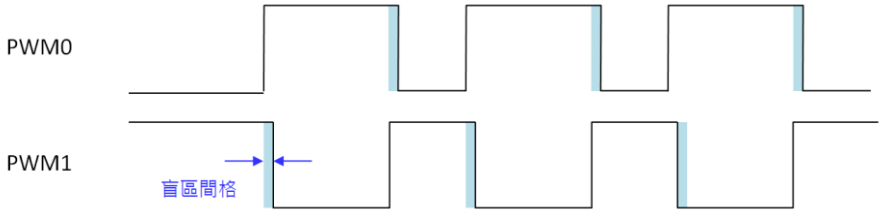


Figure 3-14: LCD_PWM [0] and LCD_PWM [1] Complementary Output Blind Spot Timing

Note: Users can refer to Section 26.1 for the PWM register instructions of the TFT LCD controller.

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3.4.7. USB Interface

LT7589 provides a set of USB interfaces with USB slave functionality. This USB interface can be used to connect data between a PC used to update the internal MCU program of LT7589 and external SPI flash memory. For more detailed information, please refer to the UI-Editor-III user manual or Chapter 24 instructions.

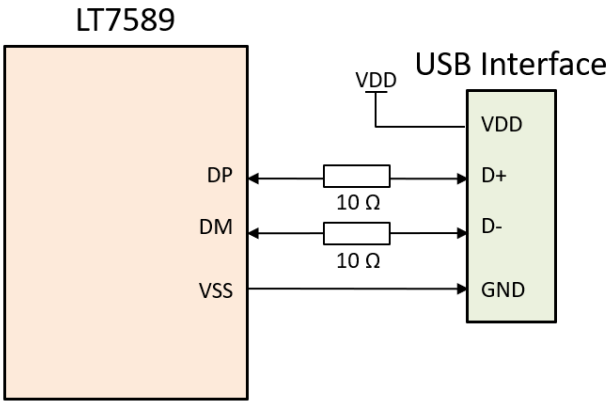


Figure 3-15: LT7589 USB Interface

3.4.8. Canbus Interface

LT7589 provides Canbus bus interfaces CANTX and CANRX. In practical applications, an external Canbus driver chip is required. Please refer to the schematic diagram below. For more information on Canbus applications, please refer to Chapter 19.

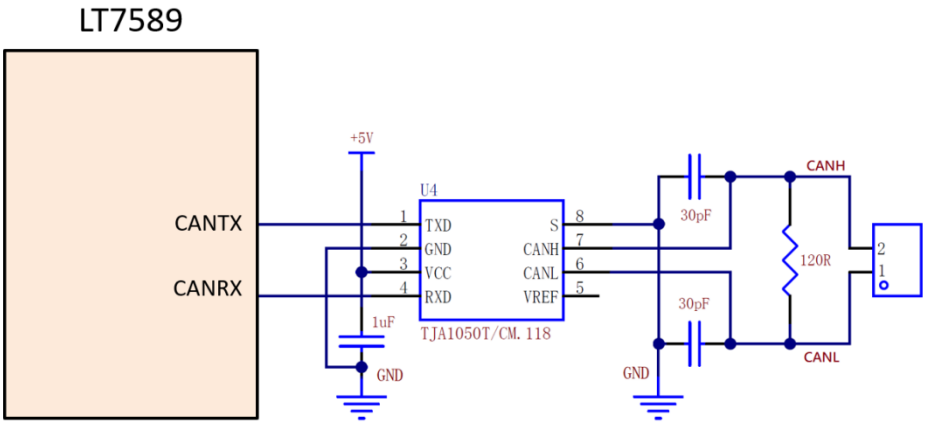


Figure 3-16: Example of Canbus Interface Application

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3.4.9. Clock Signals

3.4.9.1. MCU Clock Signals

The clock signal inside LT7589 is shown in the following figure. The MCU part includes an external 12MHz crystal oscillator circuit, and its internal PLL circuit generates a clock signal for use by CPU, SPI Flash, Uart and other circuits.

The clock of the MCU of LT7589 is set by the clock and power control module (CLKPWRM), please refer to Chapter 9 for details.

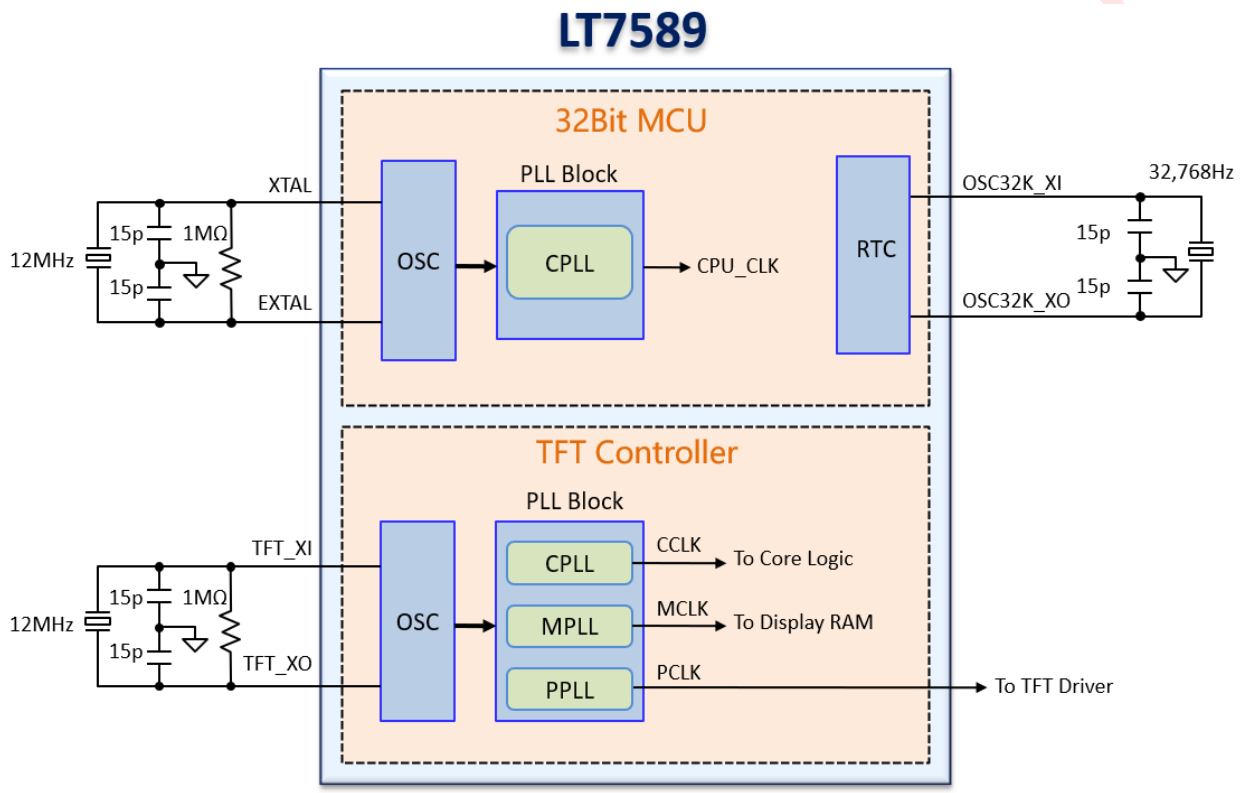


Figure 3-17: Clock Signal Structure Diagram

3.4.9.2. TFT LCD Controller Signals

The TFT LCD controller also includes an external 12MHz crystal oscillator circuit, which has three PLL circuits inside to generate clock signals for the GUI internal logic circuit, SDRAM, and external LCD driver circuit of the TFT LCD graphic display controller.

Note: The clock signal source of the TFT LCD controller can be generated by a set of PWM outputs from the MCU, or by using a 12MHz crystal oscillator signal referenced from the MCU (as shown in the figure below) to save the cost of one crystal oscillator.

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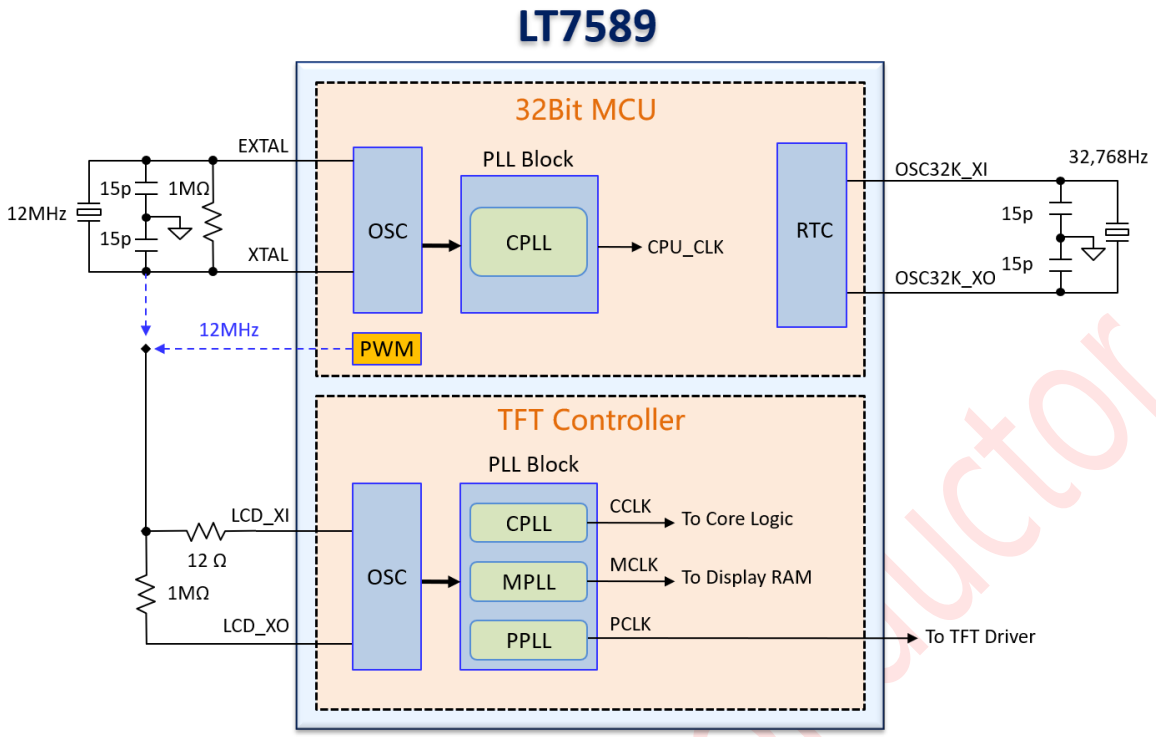


Figure 3-18: The TFT Controller Uses an External 12MHz Crystal Oscillator Circuit

3.4.9.3. RTC Clock

The LT7589 has an RTC module inside, which has independent power supply (VBAT) and a low-power 32.768KHz clock crystal oscillator (as shown in the above figure) and RTC circuit. When the external power is cut off, it can continue timing work under battery operation. Please refer to Chapter 17 Clock Controller (RTC) Description and Chapter 29 Schematic Diagram.

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3.4.10. Reset Signals

The MCU and TFT LCD controller of LT7589 have their own independent reset signals (as shown in Figure 3-19). The reset signal of MCU can be generated by a simple RC circuit. If you are concerned about instability caused by frequent power switches, it is recommended to use a reset chip to generate the reset signal (as shown in Figure 3-20).

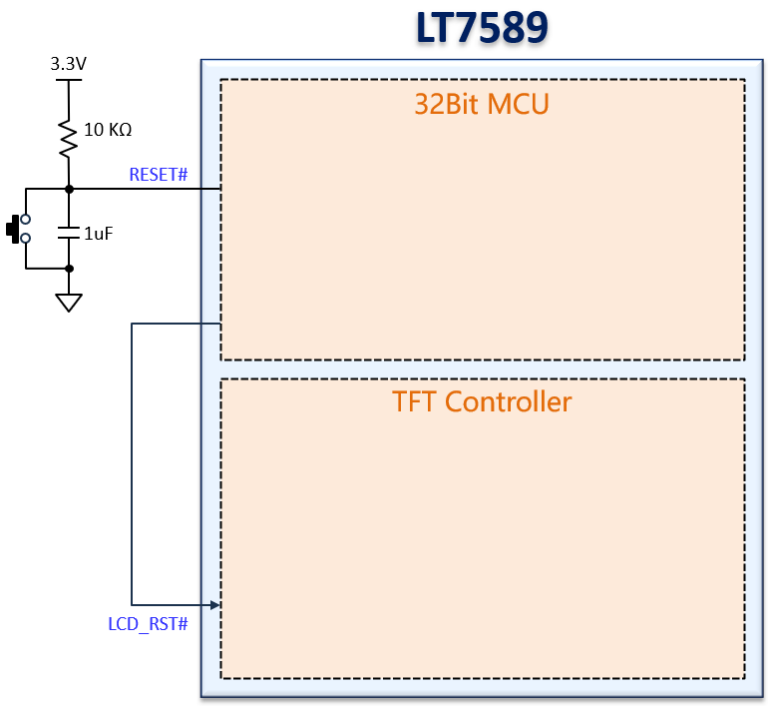


Figure 3-19: LT7589 Reset Signal Structure Diagram

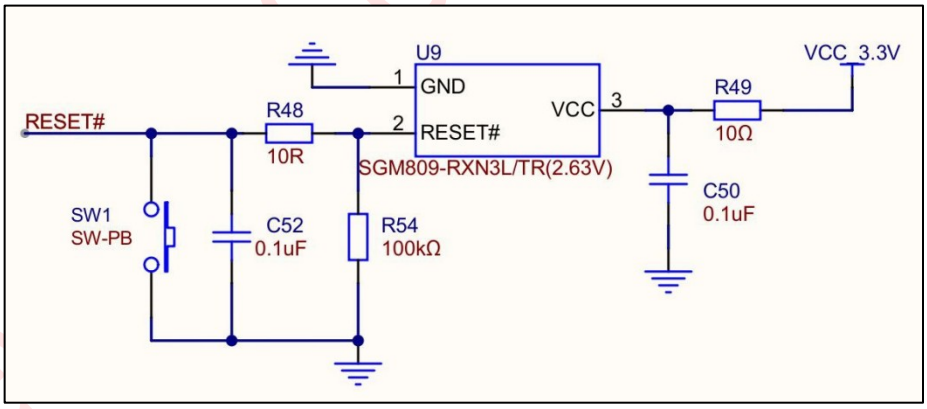


Figure 3-20: Generate Reset Signal by Reset Chip

The reset signal of TFT LCD controller can be generated by one IO port of MCU, please refer to the application circuit in Chapter 29.

The MCU of LT7589 is equipped with a reset control module (RCM), which is used to determine the reason for the reset, confirm the appropriate reset signal to the system, and then maintain a historical record of the reset reason. It can also be used to control the reset output signal RSTOUT. Please refer to Chapter 10 for details on the reset control module (RCM).

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4. 32-bits RISC Introduction

This section describes the functionality of the LT7589's 32-bits RISC microprocessor, which is based on M*Core instruction set/architecture and designed for extremely low-power and cost-sensitive embedded control applications. The architecture of this 32-bits RISC MCU is same as Levetop's 32-bits MCU – LT32U05.

For the smaller size and power dissipation, 32-bits RISC is built on a new 3-stage pipeline von Neumann architecture.

The 32-bits RISC also integrates an EIC(embedded interrupt controller) to reduce system area.

The external bus interface protocol is AHB-lite. More configurable options are available in 32-bits RISC design. By leveraging these configurable options, tradeoff among performance, functionality and cost are more flexible. The gate count of 32-bits RISC varies from 12K to 20K with different configurations.

4.1. Features

The main features of the 32-bits RISC are as follows:

- 32-bits load/store reduced instruction set computer (RISC) architecture with fixed 16-bits instruction length
- 16 entry 32-bits general-purpose register file
- Efficient 3-stage execution pipeline, hidden from application software
- Single-cycle instruction execution for many Instructions, three cycles for branches
- Support byte/halfword/word memory accesses
- Embedded interrupt controller, support nested vector interrupts and low power mode wakeup
- Single-cycle 32-bits x 32-bits hardware integer multiplier array
- 3~13 cycles hardware integer divider array
- AHB-lite external bus

4.2. Microarchitecture Summary

The 32-bits RISC utilizes a 3-stage pipeline for instruction execution. The instruction fetch, instruction decode/register file read, and execute/writeback stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

16 general-purpose registers are provided for source operands and instruction results. Register R15 is used as the link register to hold the return address for subroutine calls, and Register R0 is associated with the current stack pointer value by convention.

A dual entry 32-bits instruction buffer is provided to allow instruction prefetching to obtain two instructions per clock cycle from memory with a maximum of three buffered instructions, thus reducing or eliminating bus resource conflicts with data memory accesses. The unified bus structure is sufficient to sustain both instruction and data bandwidth requirements without resorting to expensive dual bus structures.

Memory load and store operations are provided for byte, halfword, and word (32-bits) data with automatic zero extension of byte and halfword load data These instructions can be pipelined to allow effective single cycle throughput for short sequences. Data dependent operations can complete in two clock cycles. Load and store multiple register instructions allow low overhead context save and restore operations; these instructions can be executed in (N+1) clock cycles, where N is the numbers of registers to transfer.

A single condition code/carry (C) bit is provided for condition testing and for use in implementing arithmetic and logical operations greater than 32-bits. Typically, the C bit is set only by explicit test/comparison operations, not as a side-effect of normal instruction operation. Exceptions to this rule occur for specialized operations where it is desirable to combine condition setting with actual computation.

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4.3. Programming Model

The 32-bits RISC programming model is defined separately for two privilege modes: supervisor and user. HPROT[1] bit is used to indicate the privilege modes. Programs access registers based on the indicated mode. User programs can only access registers specific to the user mode; system software executing in the supervisor mode can access all registers, using the control registers to perform supervisory functions. User programs are thus restricted from accessing privileged information, and the operating system performs management and service tasks for the user programs by coordinating their activities.

All instructions can be executed in either mode. User program can also execute stop, doze, or wait instructions. The trap #n instructions provide controlled access to operating system services for user programs. To prevent a user program from entering the supervisor mode except in a controlled manner, instructions that can alter the S-bit in the program status register (PSR) are privileged.

When the S-bit in the PSR is set, the processor executes instructions in the supervisor mode. Bus cycles associated with an instruction indicate either supervisor or user access depending on the mode.
The processor utilizes the user programming model when it is in normal user mode processing. During exception processing, the processor changes from user to supervisor mode. Exception processing saves the current value of the PSR to stack memory and then sets the S bit in the PSR, forcing the processor into the supervisor mode. To return to the previous operating mode, a system routine may execute the RTE (return from exception) instruction, causing the instruction pipeline to be flushed and refilled from the appropriate address space.

The registers depicted in the programming model (see **Figure 6-1**) provide operand storage and control. The user programming model consists of 16 general-purpose 32-bits registers, the 32-bits program counter (PC) and the Condition/Carry (C) bit. The C bit is implemented as bit 0 of the PSR. By convention, register R15 serves as the link register for subroutine calls, and register R0 is typically used as the current stack pointer.

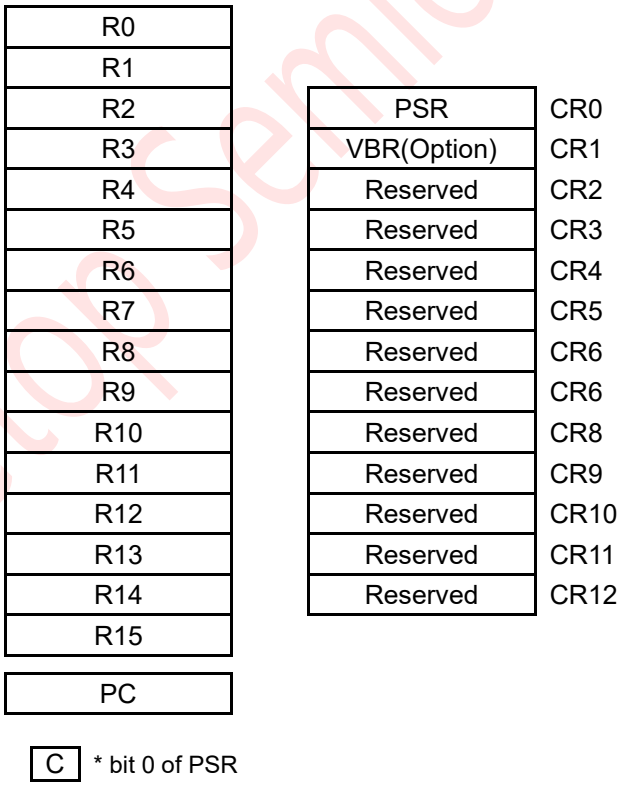


Figure 4-1: Programming Model

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4.4. Data Format Summary

The operand data formats supported by the integer unit are standard two's complement data formats. The operand size for each instruction is either explicitly encoded in the instruction (load/store instructions) or implicitly defined by the instruction operation (index operations, byte extraction). Typically, instructions operate on all 32-bits of the source operand(s) and generate a 32-bits result.

Memory may be viewed from either a Big Endian or Little Endian byte ordering perspective depending on the processor configuration (see **Figure 4-2**). In Big Endian mode (the default operating mode), the most significant byte (byte 0) of word 0 is located at address 0. For Little Endian mode, the most significant bye of word 0 is located at address 3. Within registers, bits are numbered within a word starting with bit 31 as the most significant bit (see **Figure 4-3**). By convention, byte 0 of a register is the most significant byte regardless of Endian mode. This is only an issue when executing the XTRB[0-3] instructions.

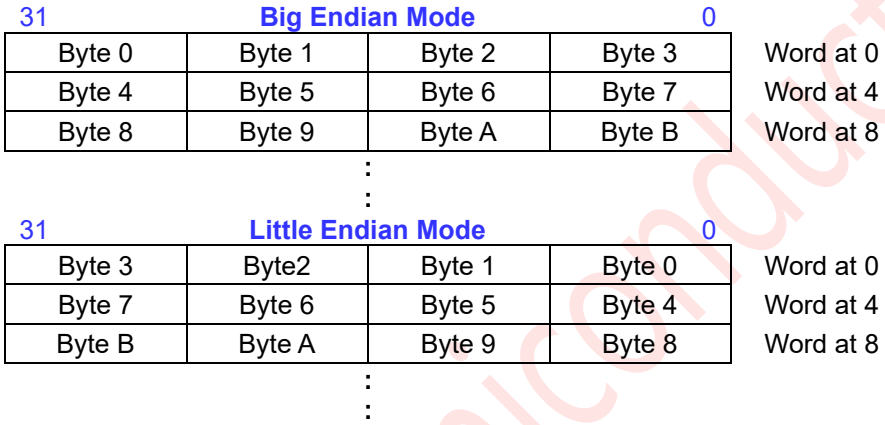


Figure 4-2: Data Organization in Memory

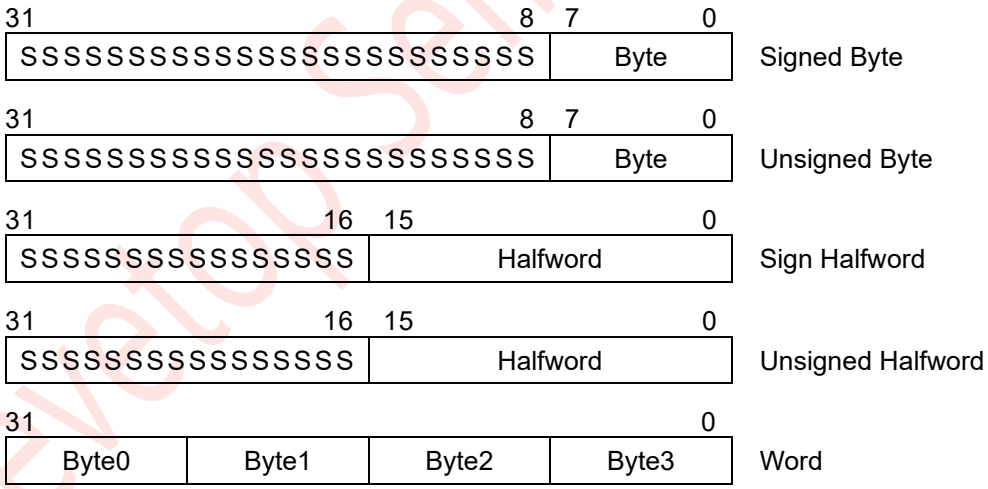


Figure 4-3: **Data Organization in Registers**

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4.5. Operand Addressing Capabilities

The 32-bits RISC accesses all memory operands through load and store instructions, transferring data between the general-purpose registers (GPRs) and memory. Register + 4-bits scaled displacement addressing mode is used for the load and store instructions to address byte, halfword, or word (32-bits) data.

Load and store multiple instructions allow a subset of the 16 GPRs to be transferred to or from a base address pointed to by register R0 (the default stack pointer by convention).

Load and store register quadrant instructions use register indirect addressing to transfer a register quadrant to or from memory.

4.6. Instruction Set Overview

The instruction set is tailored to support high-level languages and is optimized for those instructions most commonly executed. A standard set of arithmetic and logical instructions is provided as well as instruction support for bit operations, byte extraction, data movement, control flow modification, and a small set of conditionally executed instructions which can be useful in eliminating short conditional branches.

The following table provides an alphabetized listing of the 32-bits RISC instruction set.

Table 4-1: 32-bits RISC Instruction Set

Memonic	Description
ABS	Absolute Value
ADDC	Add with C bit
ADDI	Add Immediate
ADDU	Add Unsigned
AND	Logical AND
ANDI	Logical AND Immediate
ANDN	AND NOT
ASR	Arithmetic Shift Right
ASRC	Arithmetic Shift Right, update C bit
ASRI	Arithmetic Shift Right Immediate
BCLRI	Clear Bit
BF	Branch on Condition False
BGENI	Bit Generate Immediate
BGENR	Bit Generate Register
BKPT	Breakpoint
BMASKI	Bit Mask Immediate
BR	Branch
BGENI	Bit Generate Immediate
BGENR	Bit Generate Register
BKPT	Breakpoint
BMASKI	Bit Mask Immediate
BR	Branch
BREV	Bit Reverse
BSETI	Bit Set Immediate
BSR	Branch to Subroutine
BT	Branch on Condition True
BTSTI	Bit Test Immediate
CLRF	Clear Register on Condition False

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Memonic	Description
CLRT	Clear Register on Condition True
CMPHS	Compare Higher or Same
CMPLT	Compare Less-Than
CMPLTI	Compare Less-Than Immediate
CMPNE	Compare Not Equal
CMPNEI	Compare Not Equal Immediate
DECF	Decrement on Condition False
DECGT	Decrement Register and Set Condition if Result Greater-than Zero
DECLT	Decrement Register and Set Condition if Result Less-than Zero
DECNE	Decrement Register and Set Condition if Result Not Equal to Zero
DECT	Decrement On Condition True
DIVS (1)	Divide Signed Integers
DIVU (1)	Divide Unsigned Integers
DOZE	Doze
FF1 (1)	Find First One
INCF	Increment on Condition False
INCT	Increment On Condition True
IXH	Index Halfword
IXW	Index Word
JAVASW	Java interpreter switch
JMP	Jump
JMPI	Jump Indirect
JSR	Jump to Subroutine
JSRI	Jump to Subroutine Indirect
LD.[BHW]	Load
LDM	Load Multiple Registers
LDQ	Load Register Quadrant
LRW	Load Relative Word
LSL, LSR	Logical Shift Left and Right
LSLC, LSRC	Logical Shift Left and Right, update C bit
LSLI, LSRI	Logical Shift Left and Right by Immediate
MFCR	Move from Control Register
MOV	Move
MOVI	Move Immediate
MOVF	Move on Condition False
MOVT	Move on Condition True
MTCR	Move to Control Register
MULSH	Multiply signed Halfwords
MULT	Multiply
MVC	Move C bit to Register
MVCV	Move Inverted C bit to Register
NOT	Logical Complement

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Memonic	Description
OR	Logical Inclusive-OR
ROTLI	Rotate Left by Immediate
RSUB	Reverse Subtract
RSUBI	Reverse Subtract Immediate
RTE	Return from Exception
RFI	Return from Interrupt
SEXTB	Sign-extend Byte
SEXTH	Sign-extend Halfword
ST.[BHW]	Store
STM	Store Multiple Registers
STQ	Store Register Quadrant
STOP	Stop
SUBC	Subtract with C bit
SUBU	Subtract
SUBI	Subtract Immediate
SYNC	Synchronize
TRAP	Trap
TST	Test Operands
TSTNBZ	Test for No Byte Equal Zero
WAIT	Wait
XOR	Exclusive OR
XSR	Extended Shift Right
XTRB0	Extract Byte 0
XTRB1	Extract Byte 1
XTRB2	Extract Byte 2
XTRB3	Extract Byte 3
ZEXTB	Zero-extend Byte
ZEXTH	Zero-extend Halfword

Note (1) : Not implemented in the current version.

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5. Memory and Registers Map

5.1. Introduction

LT7589 中 MCU 的内建/外部内存、寄存器包括：

- 内建 2M Bytes QSPI Flash 闪存，作为存放串口屏协议代码及客户二次开发所增加或修改的代码
- 内建 8K Bytes 内部 Boot ROM
- 内建 768K Bytes 内部静态 SRAM
  - 系统 RAM：前 256K Bytes，地址由 0x00800000 开始
  - 显存 RAM：后 512K Bytes，地址由 0x00840000 开始
- 最高 128M Bytes 的外部 QSPI Flash 闪存空间
- 各模块内部寄存器

5.2. Address Map

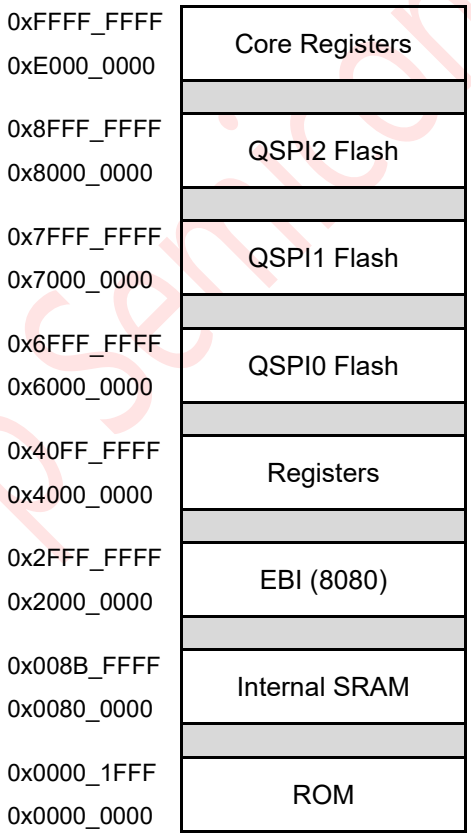


Figure 5-1: Address Map

The LT7589's Register Map and SPI's Address Map are show as following table:

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Table 5-1: Register Address Location Map

配置地址	最大区块	硬 件 模 块	参考章节
0x4000_0000	64Kbyte	Direct Memory Access Controller (DMAC)	13
0x4001_0000	64Kbyte	Chip Configuration Module (CCM)	6
0x4002_0000	64Kbyte	Reset Control Module (RCM)	10
0x4003_0000	64Kbyte	Clock and Power Control Module (CLKPWRM)	9
0x4004_0000	64Kbyte	Programmable Interrupt Timer 0 (PIT0)	15
0x4005_0000	64Kbyte	Programmable Interrupt Timer 1 (PIT1)	15
0x4006_0000	64Kbyte	Programmable Interrupt Timer 2 (PIT2)	15
0x4007_0000	64Kbyte	Programmable Interrupt Timer 3 (PIT3)	15
0x4008_0000	64Kbyte	Serial Communication Interface 1 (SCI1)	20
0x4009_0000	64Kbyte	Serial Communication Interface 0 (SCI0)	20
0x400A_0000	64Kbyte	Analog Comparator 0 (COMP0)	23
0x400B_0000	64Kbyte	Analog Comparator 1 (COMP1)	23
0x400C_0000	64Kbyte	Serial Communication Interface 2 (SCI2)	20
0x400D_0000	64Kbyte	Pulse Width Modulator 0 (PWM0)	22
0x400E_0000	64Kbyte	Pulse Width Modulator 1 (PWM1)	22
0x400F_0000	64Kbyte	Edge Port Module 0 (EPORT0)	18
0x4010_0000	64Kbyte	Edge Port Module 1 (EPORT1)	18
0x4011_0000	64Kbyte	Analog-to-Digital Convertor (ADC)	25
0x4012_0000	64Kbyte	Option Byte (OPB)	14
0x4013_0000	64Kbyte	WatchDog Timer (WDT)	16
0x4014_0000	64Kbyte	Real Time Controller (RTC)	17
0x4015_0000	64Kbyte	Reserved.	--
0x4016_0000	64Kbyte	USB2.0 Full-Speed Device Controller (USBC)	24
0x4017_0000	64Kbyte	Reserved.	--
0x4018_0000	64Kbyte	Reserved.	--
0x4019_0000	64Kbyte	CACHE Module (CACHEM)	12
0x401A_0000	64Kbyte	Reserved.	--
0x401B_0000	64Kbyte	Reserved.	--
0x401C_0000	64Kbyte	CANBus Controller (CANBC)	19
0x401D_0000	64Kbyte	Edge Port Module 2 (EPORT2)	18
0x6000_0000	64Kbyte	Synchronous Serial Interface 0 (SSI0) - QSPI0	21
0x7000_0000	64Kbyte	Synchronous Serial Interface 1 (SSI1) - QSPI1	21
0x8000_0000	64Kbyte	Synchronous Serial Interface 2 (SSI2) - QSPI2	21
0xE000_0000	4Kbyte	Embedded Interrupt Controller (EIC)	7
0xE000_1000	4Kbyte	Embedded Programmable Timer (EPT)	8

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6. Chip Configuration Module (CCM)

6.1. Introduction

The Chip Configuration Module (CCM) of LT7589 controls the chip configuration.

6.2. Features

The CCM performs below operations:

- •Configurate wakeup function
- •Configurate LDO mode
- •Configurate IO function

6.3. Memory Map and Registers

This subsection provides a description of the memory map and registers. The CCM base address is 0x4001_0000. The following table shows the offset address of CCM registers.

6.3.1. Memory Map

Table 6-1: CCM Memory Map

Offset Address	Bits[31:16]	Bits[15:0]	Access[1]
0x0000	WKUPC — Wakeup Configuration Register		S
0x0004	Reserved		S
0x0008	Reserved		S
0x000C	CPPDC — Chip Pin Pull Down Configuration Register		S
0x0010	Reserved		S
0x0014	QSPIXIPCR — QSPI XIP Mode Configuration Register		S
0x0018	Reserved		S
0x001C	QSPIKEYR — QSPI 32-Bit Key Register		S
0x0020	QSPIGPIOCR — QSPI GPIO Configuration Register		S
0x0024	MCURAMPRIOCR — MCU Access RAM Priority Configuration Register		S
0x0028	EPORT2FCR — EPORT2 Function Configuration Register		S

Note:

S = supervisor-only access. Accessing supervisor only address locations in user mode has no effect and result in a cycle termination transfer error.

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6.3.2. Register Descriptions

6.3.2.1. Wakeup Configuration Register (WKUPC)

Address: CCM_BASEADDR + 0x0000_0000

	31	30	29	28	27	26	25	24
Read: Write:	WKUPFILTEREN	WKUPSEN [30:24]						
Reset:	0	1	1	1	1	1	1	1

	23	22	21	20	19	18	17	16
Read: Write:	WKUPSEN [23:16]							
Reset:	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8
Read: Write:	WKUPSEN [15:8]							
Reset:	1	1	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
Read: Write:	WKUPSEN [7:0]							
Reset:	1	1	1	1	1	1	1	1

Figure 6-1: Wakeup Configuration Register (WKUPC)

WKUPFILTEREN — Wakeup Source Filter Enable

If the WKUPFILTEREN is set, the wakeup source will remove glith through a filter and then wakeup the chip from standby mode.

1 = Wakeup source filter is enabled

0 = Wakeup source filter is disabled

WKUPSEN[30:0] — Wakeup Source Enable

This field controls whether the corresponding source is used as a source to wakeup the chip from standby mode. If set, the corresponding source is used as a wakeup source.

Table 6-2: WKUPSEN and Corresponding Wakeup Source

WKUPSEN	Wakeup Source
WKUPSEN[30]	INT2[3]
WKUPSEN[29]	INT2[2]
WKUPSEN[28]	INT2[1]
WKUPSEN[27]	RTC Interrupt
WKUPSEN[26]	PVD Interrupt
WKUPSEN[25]	USB Resume
WKUPSEN[24]	COMP1 Interrupt
WKUPSEN[23]	COMP0 Interrupt
WKUPSEN[22]	INT2[6]
WKUPSEN[21]	INT2[5]

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WKUPSEN	Wakeup Source
WKUPSEN[20]	I2C
WKUPSEN[19]	WDT0 Interrupt
WKUPSEN[18]	JTAG POWER ON REQUEST
WKUPSEN[17]	RESET# Pin
WKUPSEN[16]	WDT0 Reset
WKUPSEN[15]	INT1[7]
WKUPSEN[14]	INT1[6]
WKUPSEN[13]	INT1[5]
WKUPSEN[12]	INT1[4]
WKUPSEN[11]	INT1[3]
WKUPSEN[10]	INT1[2]
WKUPSEN[9]	INT1[1]
WKUPSEN[8]	INT1[0]
WKUPSEN[7]	INT0[7]
WKUPSEN[6]	INT0[6]
WKUPSEN[5]	INT0[5]
WKUPSEN[4]	INT0[4]
WKUPSEN[3]	INT0[3]
WKUPSEN[2]	INT0[2]
WKUPSEN[1]	INT0[1]
WKUPSEN[0]	INT0[0]

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6.3.2.2. Chip Pin Pull Down Configuration Register (CPPDC)

Address: CCM_BASEADDR + 0x0000_000C

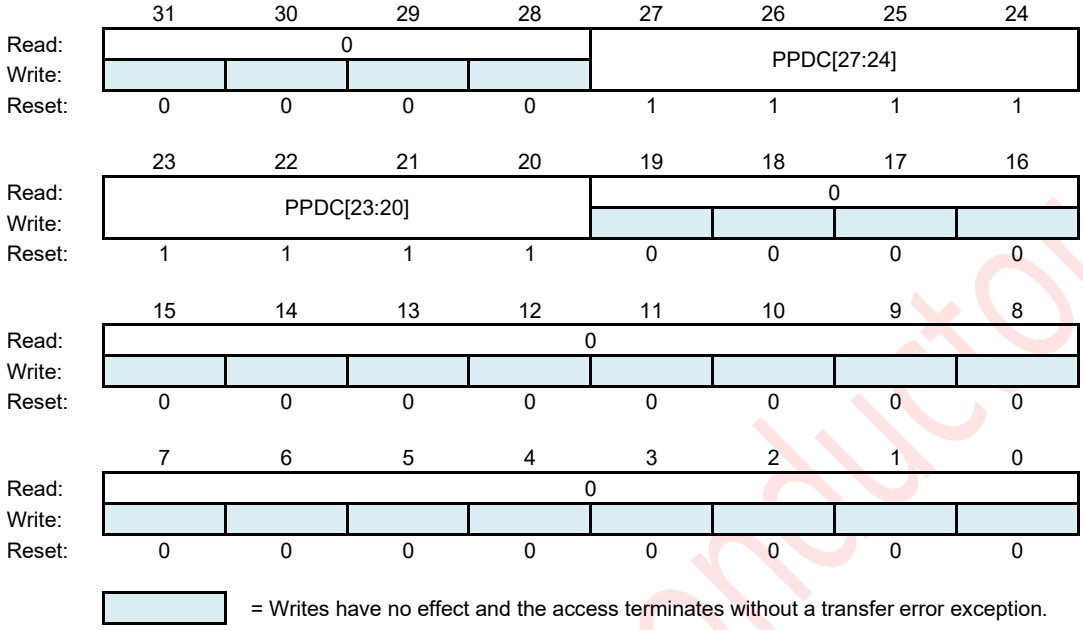


Figure 6-2: Chip Pin Pull Down Configuration Register (CPPDC)

PPDC[27:20] — Pin Pull Down Configuration Field

This read/write field controls the pull down function of the corresponding pin which shows in following table.

1 = Pull down function of the corresponding pin is enabled

0 = Pull down function of the corresponding pin is disabled

Table 6-3: Chip Pin Pull Down Configuration

Pin Name	Pull Down Configuration Bit	Pull Down Function
PWM0[3]	PPDC[27]	0: Disable, 1: Enable
PWM0[2]	PPDC[26]	0: Disable, 1: Enable
PWM0[1]	PPDC[25]	0: Disable, 1: Enable
PWM0[0]	PPDC[24]	0: Disable, 1: Enable
PWM1[3]	PPDC[23]	0: Disable, 1: Enable
PWM1[2]	PPDC[22]	0: Disable, 1: Enable
PWM1[1]	PPDC[21]	0: Disable, 1: Enable
PWM1[0]	PPDC[20]	0: Disable, 1: Enable

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6.3.2.3. QSPI XIP Mode Configuration Register (QSPIXIPMCFR)

The QSPIXIPMCFR register is a read-writable register.

Address: CCM_BASEADDR + 0x0000_0014

	31	30	29	28	27	26	25	24
Read:	0						QSPI2_DATA_ENCR_EN	QSPI2_XIPEN
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0						QSPI1_DATA_ENCR_EN	QSPI1_XIPEN
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0						QSPI0_DATA_ENCR_EN	QSPI0_XIPEN
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 6-3: QSPI XIP Mode Configuration Register (QSPIXIPMCFR)

QSPIx_DATA_ENCR_EN — QSPIx XIP Transfer Data Encrypt function Enable Control bit

1 = QSPIx XIP Transfer Data Encrypt function is Enabled
0 = QSPIx XIP Transfer Data Encrypt function is Disabled

QSPIx_XIPEN — QSPIx XIP Mode Enable Control bit

1 = QSPIx XIP Mode is Enabled
0 = QSPIx XIP Mode is Disabled

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6.3.2.4. QSPI 32-Bit Key Register (QSPILKEYR)

The QSPIKEYR register is a writable register, and always returns 0's when being read..

Address: CCM_BASEADDR + 0x0000_001C

	31	30	29	28	27	26	25	24
Read:	0							
Write:	QSPI_KEY[31:24]							
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0	0	0	0	0	0	0	0
Write:	QSPI_KEY[23:16]							
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0	0	0	0	0	0	0	0
Write:	QSPI_KEY[15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0	0	0	0	0	0	0	0
Write:	QSPI_KEY[7:0]							
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 6-4: QSPI 32-Bit Key Register (QSPILKEYR)

6.3.2.5. QSPI GPIO Configuration Register (QSPIGPIOCR)

The QSPIGPIOCR register is a read-writable register.

Address: CCM_BASEADDR + 0x0000_0020

	31	30	29	28	27	26	25	24
Read:	QSPI2_SS_GPIOEN	QSPI1_SS_GPIOEN	QSPI0_SS_GPIOEN	0		QSPI2_SS_PUE	QSPI1_SS_PUE	QSPI0_SS_PUE
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0					QSPI2_SS_OBE	QSPI1_SS_OBE	QSPI0_SS_OBE
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0					QSPI2_SS_DO	QSPI1_SS_DO	QSPI0_SS_DO
Write:								
Reset:	0	0	0	0	0	1	1	1

	7	6	5	4	3	2	1	0
Read:	0					QSPI2_SS_DI	QSPI1_SS_DI	QSPI0_SS_DI
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 6-5: QSPI GPIO Configuration Register (QSPIGPIOCR)

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QSPIx_SS_GPIOEN — QSPIx CS# Pin GPIO Mode Enable Control bit

1 = QSPIx CS# Pin GPIO Mode Is enabled

0 = QSPIx CS# Pin GPIO Disabled

QSPIx_SS_PUE — QSPIx CS# Pin Pullup Enable Control bit in GPIO Input Mode.

Note: QSPI2_SS_PUE is not valid for LT7589.

1 = QSPIx CS# Pin GPIO Pullup Is enabled

0 = QSPIx CS# Pin GPIO Pullup Disabled

QSPIx_SS_OBE — QSPIx CS# Pin Output Enable Control bit in GPIO Mode

1 = QSPIx CS# Pin GPIO Output Is enabled

0 = QSPIx CS# Pin GPIO Output Disabled

QSPIx_SS_DO — QSPIx CS# Pin Output Data in GPIO Output Mode

1 = QSPIx CS# will be driven High in GPIO Output Mode

0 = QSPIx CS# will be driven Low in GPIO Output Mode

QSPIx_SS_DI — QSPIx CS# Pin value in GPIO Mode

1 = Indicated QSPIx CS# Pin is High level in GPIO Input Mode

0 = Indicated QSPIx CS# Pin is Low level in GPIO Input Mode

6.3.2.6. MCU Access RAM Priority Configuration Register (MCURAMPRIOCR)

The MCURAMPRIOCR register is a read-writable register.

Address: CCM_BASEADDR + 0x0000_0024

	31	30	29	28	27	26	25	24
Read: / Write:	RAMPRIOTEST[1:0]		CACHERAMPD	DISPLAYRAMPD	SYSRAM3PD	SYSRAM2PD	SYSRAM1PD	SYSRAM0PD
Reset:	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
Read: / Write:	0		CACHERAMISOEN	DISPLAYRAMISOEN	SYSRAM3ISOEN	SYSRAM2ISOEN	SYSRAM1ISOEN	SYSRAM0ISOEN
Reset:	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
Read: / Write:	0							
Reset:	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
Read: / Write:	0						RAM256KP	RAM512KP
Reset:	0	0	0	0	0	0	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 6-6: MCU Access RAM Priority Configuration Register (MCURAMPRIOCR)

RAMPRIOTEST[1:0] — MCURAMPRIOCR Write Access Sequence In

The writable bit of MCURAMPRIOCR register cannot be changed, unless the correct sequence is written. The right sequence is: 2'b01 → 2'b10 → 2'b11. After these two bits are written by this sequence, these two bits' value == 2'b11, then the writable bit of MCURAMPRIOCR register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

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CACHERAMPD — The power supply of Cache RAM will be shut-down when writing 1'b1 to it.

DISPLAYRAMPD — Please refer to CACHERAMPD bit description.

SYSRAM3PD — Please refer to CACHERAMPD bit description.

SYSRAM2PD — Please refer to CACHERAMPD bit description.

SYSRAM1PD — Please refer to CACHERAMPD bit description.

SYSRAM0PD — Please refer to CACHERAMPD bit description.

CACHERAMISOEN — Cache RAM output value will be isolated when writing 1'b1 to it.

Note: Cache RAM output should be isolated before the power of Cache RAM is shut-off to avoid leakage current.

DISPLAYRAMISOEN — Please refer to CACHERAMISOEN bit description.

SYSRAM3ISOEN — Please refer to CACHERAMISOEN bit description.

SYSRAM2ISOEN — Please refer to CACHERAMISOEN bit description.

SYSRAM1ISOEN — Please refer to CACHERAMISOEN bit description.

SYSRAM0ISOEN — Please refer to CACHERAMISOEN bit description.

RAM256KP — MCU Accesses System RAM256K Priority Configuration Register
This bit determines whether MCU has higher priority when MCU and Blender access System RAM256K at the same time.

1 = MCU has higher priority when MCU and Blender access System RAM256K at the same time.

0 = MCU has lower priority when MCU and Blender access System RAM256K at the same time.

RAM512KP — MCU Accesses Display RAM512K Priority Configuration Register

This bit determines whether MCU has higher priority when MCU and Blender access Display RAM512K at the same time.

1 = MCU has higher priority when MCU and Blender access Display RAM512K at the same time.

0 = MCU has lower priority when MCU and Blender access Display RAM512K at the same time.

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6.3.2.7. EPORT2 Function Configuration Register (EPORT2FCR)

The EPORT2FCR register is a read-writable register.

Address: CCM_BASEADDR + 0x0000_0028

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	EPORT2EN[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 6-7: EPORT2 Function Configuration Register (EPORT2FCR)

EPORT2EN[7:0] — EPORT2 Function Enable control bit.

Table 6-4: EPORT2 Function Control Bit

EPORT2 Enable Bit	1'b1	1'b0
EPORT2EN[7]	INT2[7]	CANRX
EPORT2EN[6]	INT2[6]	CANTX
EPORT2EN[5]	INT2[5]	RXD2
EPORT2EN[4]	INT2[4]	TXD2
EPORT2EN[3]	INT2[3]	RXD1
EPORT2EN[2]	INT2[2]	TXD1
EPORT2EN[1]	INT2[1]	RXD0
EPORT2EN[0]	INT2[0]	TXD0

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7. Embedded Interrupt Controller(EIC)

This section describes the Embedded Interrupt Controller of the 32-bits RISC.

7.1. Introduction

LT7589 has an Interrupt Controller that collects requests from multiple interrupt sources and provides an interface to the CPU interrupt logic.

7.2. Features

The features of the Interrupt Controller include:

- Configurable interrupt sources, up to 32
- 32 unique programmable priority levels for each interrupt source
- Independent enable/disable of pending interrupts based on priority level
- A fixed vector number for each interrupt source
- Support both level-sensitive and pulse interrupts
- Support PendTrap function
- Support Software reset

7.3. Memory Map and Registers

This subsection describes the memory map (see **Table 7-1**) and registers. The Embedded Interrupt Controller base address is 0xE000_0000.

7.3.1. Memory Map

EIC module base address(EIC_BASEADDR) is defined in 32-bits RISC internal parameter. The default value is **0xE0000000**. The EIC registers actual address is EIC_BASEADDR plus the offset address of each EIC registers. The core internal modules occupies 64K address area. The system should avoid mapping the other registers to the area from EIC_BASEADDR to EIC_BASEADDR + 0x0000_FFFF.

Table 7-1: Interrupt Controller Module Memory Map

Offset Address	Bits[31-24]	Bits[23-16]	Bits[15-8]	Bits[7-0]	Access(1)
0x0000_0000	Interrupt control status register (ICSR)				S/U
0x0000_0004	Reserved				S/U
0x0000_0008	Reserved				S/U
0x0000_000C	Reserved				S/U
0x0000_0010	Interrupt Enable Register (IER)				S/U
0x0000_0014	Reserved				S/U
0x0000_0018	Interrupt Pending Set Register (IPSR)				S/U
0x0000_001C	Interrupt Pending Clear Register (IPCR)				S/U
0x0000_0020 through 0x0000_003C	Unimplemented(2)				-
Priority level select registers (PLSR0-PLSR31)					
0x0000_0040	PLSR3	PLSR2	PLSR1	PLSR0	S/U

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Offset Address	Bits[31-24]	Bits[23-16]	Bits[15-8]	Bits[7-0]	Access(1)
0x0000_0044	PLSR7	PLSR6	PLSR5	PLSR4	S/U
0x0000_0048	PLSR11	PLSR10	PLSR9	PLSR8	S/U
0x0000_004C	PLSR15	PLSR14	PLSR13	PLSR12	S/U
0x0000_0050	PLSR19	PLSR18	PLSR17	PLSR16	S/U
0x0000_0054	PLSR23	PLSR22	PLSR21	PLSR20	S/U
0x0000_0058	PLSR27	PLSR26	PLSR25	PLSR24	S/U
0x0000_005C	PLSR31	PLSR30	PLSR29	PLSR28	S/U
0x0000_0060	System Priority level select register(SYSPLSR)				S/U
0x0000_0064 through 0x0000_007C	Unimplemented(2)				-

Notes:

(1) In 32-bits RISC, the register can be accessed in any case.

(2) Accessing to unimplemented address locations have no effect and will result in a cycle termination transfer error.

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7.3.2. Register Descriptions

This subsection contains a description of the interrupt controller module registers. The Embedded Interrupt Controller base address (**EIC_BASEADDR**) is 0xE000_0000.

7.3.2.1. Interrupt Control Status Register (ICSR)

The 32-bits interrupt control register (ICSR) reflects the state of the interrupt controller

Address: EIC_BASEADDR + 0x0000_0000

	31	30	29	28	27	26	25	24
Read:	SRST	0		SetPTrap	ClrPTrap	0		
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0	VEC[6:0]						
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-1: Interrupt Control Status Register (ICSR)

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SRST — Software Reset Bit

The write-only bit is used to create a software reset request. Setting this bit will generate a pulse on SYSRESETREQ signal. Reads always return 0.

SetPTrap — Set PendTrap Bit

The read/write bit is used to create a pending software interrupt. The action is similar to execute “trap” instruction. However, the pending software interrupt will not be entered until all the higher priority exceptions/interrupts exit. When the software interrupt entered, the bit will be cleared automatically. Reset also clears this bit.

On reads:
1 = the software interrupt is pending
0 = the software interrupt is not pending

On writes:
1 = set software interrupt to pending
0 = no effect

ClrPTrap — Clear PendTrap Bit

The read/write ClrDSI bit is used to cancel the pending software interrupt(PendTrap).
Reset clears this bit.

On reads:
1 = the software interrupt is pending
0 = the software interrupt is not pending

On writes:
1 = cancel the pending software interrupt
0 = no effect

VEC[6:0] — Interrupt Vector Number Field

The read-only VEC[6:0] field contains the 7-bits interrupt vector number. Reset clears VEC[6:0].

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7.3.2.2. Interrupt Enable Register (IER)

The read/write, 32-bits Interrupt Enable Register (IER) individually enables any current pending interrupts which are assigned to each priority level as a normal interrupt source. Enabling an interrupt source which has an asserted request causes that request to become pending, and a request to the CPU is asserted if not already outstanding.

Address: EIC_BASEADDR + 0x0000_0010

	31	30	29	28	27	26	25	24
Read: Write:	IE[31:24]							
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read: Write:	IE[23:16]							
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read: Write:	IE[15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	IE[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 7-2: Interrupt Enable Register (IER)

IE[31:0] — Interrupt Enable Field

The read/write IE[31:0] field enables interrupt requests from sources at the corresponding priority level as interrupt requests. Reset clears IE[31:0].

1 = interrupt request is enabled

0 = interrupt request disabled

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7.3.2.3. Interrupt Pending Set Register (IPSR)

Address: EIC_BASEADDR + 0x0000_0018

	31	30	29	28	27	26	25	24
Read: Write:	SetPend[31:24]							
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read: Write:	SetPend[23:16]							
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read: Write:	SetPend[15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	SetPend[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 7-3: Interrupt Pending Set Register (IPSR)

SetPend[31:0] — Interrupt Pending Set Field

The read/write SetPend[31:0] field set pending to associated interrupt and indicate whether the associated interrupt is pending . Reset clears SetPend[31:0].

On reads:

1 = the associated interrupt is pending

0 = the associated interrupt is not pending

On writes:

1 = change the state of associated interrupt to pending

0 = no effect

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7.3.2.4. Interrupt Pending Clear Register (IPCR)

Address: EIC_BASEADDR + 0x0000_001C

	31	30	29	28	27	26	25	24
Read: Write:	ClrPend[31:24]							
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read: Write:	ClrPend [23:16]							
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read: Write:	ClrPend [15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	ClrPend [7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 7-4: Interrupt Pending Clear Register (IPCR)

ClrPend[31:0] — Interrupt Pending Clear Field

The read/write ClrPend[31:0] field clear pending to associated interrupt and indicate whether the associated interrupt is pending . Reset clears ClrPend[31:0].

On reads:
1 = the associated interrupt is pending
0 = the associated interrupt is not pending

On writes:
1 = change the state of associated interrupt to not pending
0 = no effect

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7.3.2.5. Priority Level Select Registers (PLSR)

The read/write 8-bits Priority Level Select Registers (PLSRx) are 32 read/write, 8-bits priority level select registers PLSR0–PLSR31, one for each of the interrupt source. The PLSRx register assigns a priority level to interrupt source x.

Address: EIC_BASEADDR + 0x0000_0040 through EIC_BASEADDR + 0x0000_005C

	7	6	5	4	3	2	1	0
Read:	PLSRx[7:6]		0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 7-5: Priority Level Select Registers (PLSR0-PLSR31)

PLSRx[7:6] — Priority Level Select Field

IRQ0~31 has a default priority value 0~31. The lower the value, the higher the priority. This means IRQ0 priority > IRQ1 > ……. > IRQ31 as default. However, user can set PLSRx[7:6] to adjust the interrupt priority. The actual value of priority level is the default value plus PLSRx[7:6] *64. For instance, if PLSR1[7:6] = 2, IRQ1's priority value is 1 + 2*64 = 129, then IRQ1's priority is lower than any IRQ with lower priority value.

Table 7-2: Priority Value Adjustment

PLSRx[7:6]	Priority Value to be increased
00	0
01	64
10	128
11	192

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7.3.2.6. System Priority Level Select Registers (SYSPLSR)

Address: EIC_BASEADDR + 0x0000_0060

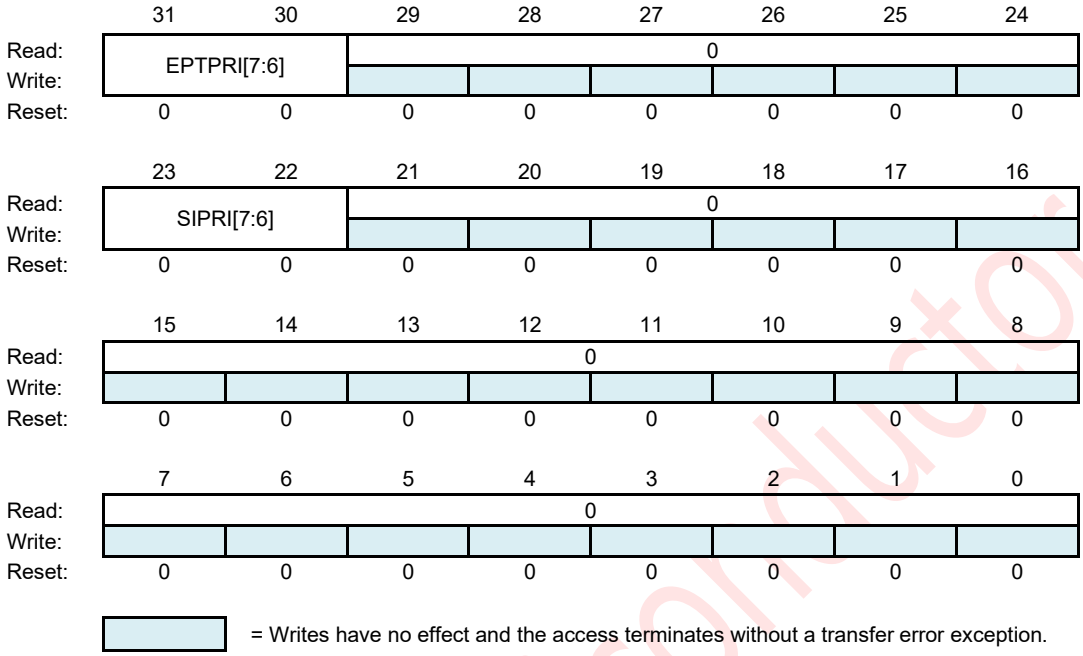


Figure 7-6: System Priority Level Select Registers (SYSPLSR)

EPTPRI[7:6] — EPT Priority Level Select Field

EPT interrupt's default priority is -2. This means EPT interrupt priority is higher than other normal IRQs and system software interrupt(PendTrap) as default. The lower the value, the higher the priority. However, user can set EPTPRI[7:6] to adjust the EPT interrupt priority. The actual value of priority level is the default value plus PRI[7:6] *64. For instance, if PRI[7:6] = 2, EPT interrupt priority value is -2 + 2*64 = 126.

Table 7-3: Priority Value Adjustment

EPTPRI[7:6]	Priority Value to be increased
00	0
01	64
10	128
11	192

SIPRI[7:6] — Software Interrupt Priority Level Select Field

Software interrupt(PendTrap) default priority is -1 . This means EPT interrupt priority is higher than other normal IRQs as default. The lower the value, the higher the priority. However, users can set SIPRI[7:6] to adjust the software interrupt priority. The actual value of priority level is the default value plus SIPRI[7:6] *64. For instance, if SIPRI[7:6] = 2, software interrupt priority value is -1 + 2*64 = 127.

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Table 7-4: Priority Value Adjustment

SIPRI[7:6]	Priority Value to be increased
00	0
01	64
10	128
11	192

7.4. Function Description

EIC supports both level-sensitive and pulse interrupts. The interrupt source number is from 1 to 32.

The interrupt will become pending by one of the following reasons:

- The EIC detects that the interrupt signal is active and the corresponding interrupt is not active
- The EIC detects a rising edge on the interrupt signal

The pending interrupt remains pending until one of the followings:

- The processor enters the ISR for the interrupt. This changes the state of the interrupt from pending to active. Then:
  – For a level-sensitive interrupt, when the processor returns from the ISR, the EIC samples the interrupt signal. If the signal is asserted, the state of the interrupt changes to pending, which might cause the processor to immediately re-enter the ISR. Otherwise, the state of the interrupt changes to inactive.

  – For a pulse interrupt, the EIC will monitor the interrupt signal continuously. If the interrupt signal is pulsed, the state of the interrupt changes to pending and active. In this case, when the processor returns from the ISR the state of the interrupt changes to pending, which might cause the processor to immediately re-enter the ISR. If the interrupt signal is not pulsed while the processor is in the ISR, when the processor returns from the ISR the state of the interrupt changes to inactive.

- Software writes to the corresponding interrupt Pending Clear Register bit.

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7.4.1. Interrupt Handling Without Confliction

If an interrupt is pulsed, the state of the interrupt changes to pending. Without confliction, the interrupt causes the processor to immediately enter the ISR. When the processor returns from the ISR, the state of the interrupt changes to inactive.

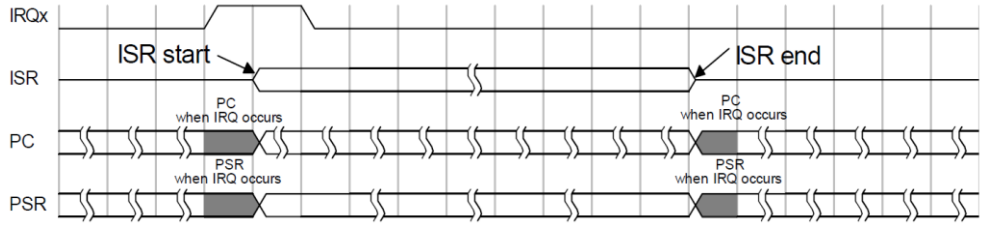


Figure 7-7: One Pulse Interrupt without Confliction

For a level-sensitive interrupt, the state of the interrupt changes to pending if the signal is asserted. Without confliction, the interrupt causes the processor to immediately enter the ISR. When the processor returns from the ISR, EIC continues to sample the interrupt signal. If the signal is not cleared, the processor will re-enter the ISR. Otherwise, the state of the interrupt changes to inactive.

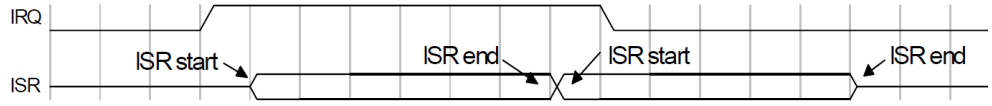


Figure 7-8: Level-sensitive Interrupt without Confliction

7.4.2. Interrupt With Confliction

When two interrupt signals are asserted at the same time, the Interrupt Arbiter will judge which one has the greater priority. For instance, if the priority of IRQx is greater than IRQy, the processor will enter ISRx and IRQy becomes pending. After the processor returns from ISRx, the processor will enter ISRy immediately.

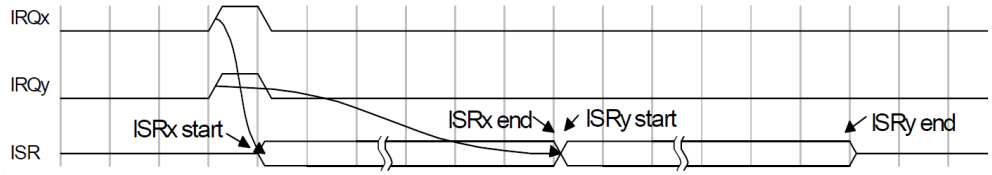
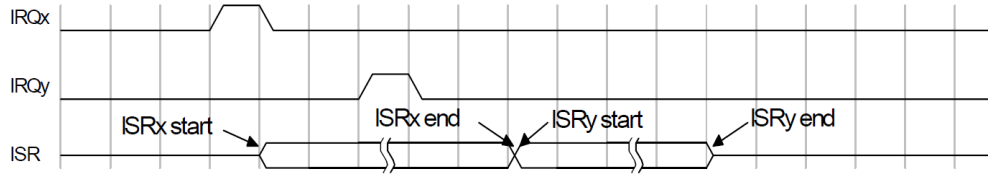


Figure 7-9: Two Interrupts Occur at the Same Time

If an interrupt signal is asserted during another interrupt handling, then there will be two cases:

1. The asserted interrupt priority is lower than the handling interrupt priority. In this case, the asserted interrupt state is pending until the handling interrupt ends.
2. The asserted interrupt priority is higher than the handling interrupt priority. In this case, the higher priority interrupt handling will be nested in the lower priority interrupt routine.



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Figure 7-10: A lower Priority Interrupt Asserted with Confliction

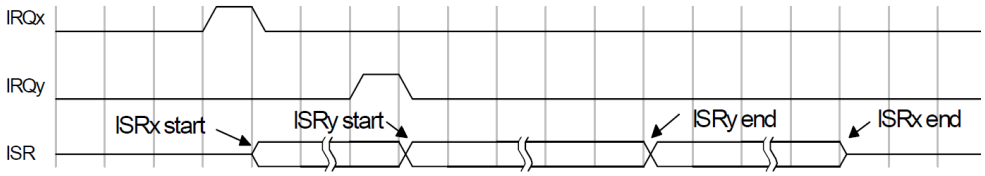


Figure 7-11: A higher Priority Interrupt Asserted with Confliction

7.4.3. Pend Trap Function

SetPTrap/ClrPTrap bits in ICSR are used to create/cancel a “pending” software interrupt request while a higher priority interrupt is handling .As soon as the processor returns from the higher priority interrupt, the “pending” software interrupt will be accepted by the processor.

Usually, Pend Trap function is used for OS task passive switch .

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7.5. Interrupts

The interrupt controller assigns a number to each interrupt source, as **Table 7-5** shows.

Table 7-5: Interrupt Source Assignment

Source	Module	Flag	Source Description	Flag Clearing Mechanism
0	ADC			
1	QSPI0	XRXOIS	XIP Receive FIFO Overflow Interrupt	
		RXFIS	Receive FIFO Full Interrupt	
		RXOIS	Receive FIFO Overflow Interrupt	
		RXUIS	Receive FIFO Underflow Interrupt	
		TXOIS	Transmit FIFO Overflow Interrupt	
		TXEIS	Transmit FIFO Empty Interrupt	
2	SCI0	TDRE	Transmit Data Register Empty Flag	
		TC	Transmission Complete	
		TXOF	Transmitter Buffer Overflow Flag	
		LBKDIF	LIN Break Detect Interrupt Flag	
		IDLE	Idle Line Flag	
		RXEDGIF	RXD0 Pin Active Edge Interrupt Flag	
		RDRF	Receive Data Register Full Flag	
		MA1F	Match 1 Flag	
		MA2F	Match 2 Flag	
		OR	Receiver Overrun Flag	
		NF	Noise Flag	
		FE	Framing Error Flag	
		PF	Parity Error Flag	
		RXUF	Receiver Buffer Underflow Flag	
3	COMP0	CPRIF		
		CPFIF		
4	COMP1	CPRIF		
		CPFIF		
5	DMAC	DONE[0]		Write DONE[0] = 1
		DONE[1]		Write DONE[1] = 1
		DONE[14]		Write DONE[14] = 1
		DONE[15]		Write DONE[15] = 1
		DMA_ESR[GPE]	Group Priority Error	Write channel number to CERR[6:0] to clear error status

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Source	Module	Flag	Source Description	Flag Clearing Mechanism
		DMA_ESR[CPE]	Channel Priority Error	Write channel number to CERR[6:0] to clear error status
		DMA_ESR[SAE]	Source Address Error	Write channel number to CERR[6:0] to clear error status
		DMA_ESR[SOE]	Source Offset Error	Write channel number to CERR[6:0] to clear error status
		DMA_ESR[DAE]	Destination Address Error	Write channel number to CERR[6:0] to clear error status
		DMA_ESR[DOE]	Destination Offset Error	Write channel number to CERR[6:0] to clear error status
		DMA_ESR[NCE]	Nbytes/Citer Configuration Error	Write channel number to CERR[6:0] to clear error status
		DMA_ESR[SGE]	Scatter/Gather Configuration Error	Write channel number to CERR[6:0] to clear error status
		DMA_ESR[SBE]	Source Bus Error	Write channel number to CERR[6:0] to clear error status
		DMA_ESR[DBE]	Destination Bus Error	Write channel number to CERR[6:0] to clear error status
6	WDT0	IF		
7	PWM0	PIFR[0]		
		PIFR[1]		
		PIFR[2]		
		PIFR[3]		
8	PWM1	PIFR[0]		
		PIFR[1]		
		PIFR[2]		
		PIFR[3]		
9	PIT0	PIF	PIT Flag	Writing a 1 to it or writing to PMR
10	PIT1	PIF	PIT Flag	Writing a 1 to it or writing to PMR
11	PIT2	PIF	PIT Flag	Writing a 1 to it or writing to PMR
12	PIT3	PIF	PIT Flag	Writing a 1 to it or writing to PMR
13	RTC	Day_intf	Day pulse flag	
		Hou_intf	Hour pulse flag	
		Min_intf	Minute pulse flag	
		Sec_intf	Second pulse flag	
		Ala_intf	Alarm flag	
		1KHz_intf	1KHz pulse flag	
		32KHz_intf	32KHz pulse flag	
14	USB_DEV	USB_DEV Flag	USB_DEV Flag	
15	I2C	I2C Flag	I2C Flag	
16	EPORT2	EPF0	Edge port 2 flag 0	Write EPF0 = 1
		EPF1	Edge port 2 flag 1	Write EPF1 = 1
		EPF2	Edge port 2 flag 2	Write EPF2 = 1

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Source	Module	Flag	Source Description	Flag Clearing Mechanism
		EPF3	Edge port 2 flag 3	Write EPF3 = 1
		EPF4	Edge port 2 flag 4	Write EPF4 = 1
		EPF5	Edge port 2 flag 5	Write EPF5 = 1
		EPF6	Edge port 2 flag 6	Write EPF6 = 1
		EPF7	Edge port 2 flag 7	Write EPF7 = 1
17	PVD	PVDO	PVD Flag	
18	CANBUS	CAN_IFRH[BUF63:BUF0]	CAN buffers 63–0 interrupts	This bit is cleared by writing it to '1'
19	CANBUS	CAN_ESR[BOFF_INT]	CANBus off interrupt	This bit is cleared by writing it to '1'
20	CANBUS	CAN_ESR[ERR_INT]	CAN error interrupt	This bit is cleared by writing it to '1'
21	CANBUS	CAN_ESR[TWRN_INT]	CAN transmit warning interrupt	This bit is cleared by writing it to '1'
22	CANBUS	CAN_ESR[RWRN_INT]	CAN receive warning interrupt	This bit is cleared by writing it to '1'
23	CANBUS	CAN_ESR[WKUP_INT]	Wake Up Interrupt	This bit is cleared by writing it to '1'
24	BLENDE	INT_END	Transfer Complete	
		INT_OQ	One quarter of the blending operation of the currently data source is completed	
		INT_HALF	Halt of the blending operation of the currently data source is completed	
25	RGBC	INTV	The completion flag of one frame transmission	
		INTN	Transmission completion flag for the specified number of frames	
26	QSPI1	XRXOIS	XIP Receive FIFO Overflow Interrupt	
		RXFIS	Receive FIFO Full Interrupt	
		RXOIS	Receive FIFO Overflow Interrupt	
		RXUIS	Receive FIFO Underflow Interrupt	
		TXOIS	Transmit FIFO Overflow Interrupt	
		TXEIS	Transmit FIFO Empty Interrupt	
27	QSPI2	XRXOIS	XIP Receive FIFO Overflow Interrupt	
		RXFIS	Receive FIFO Full Interrupt	
		RXOIS	Receive FIFO Overflow Interrupt	
		RXUIS	Receive FIFO Underflow Interrupt	

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Source	Module	Flag	Source Description	Flag Clearing Mechanism
		TXOIS	Transmit FIFO Overflow Interrupt	
		TXEIS	Transmit FIFO Empty Interrupt	
28	SCI1	TDRE	Transmit Data Register Empty Flag	
		TC	Transmission Complete	
		TXOF	Transmitter Buffer Overflow Flag	
		LBKDIF	LIN Break Detect Interrupt Flag	
		IDLE	Idle Line Flag	
		RXEDGIF	RXD1 Pin Active Edge Interrupt Flag	
		RDRF	Receive Data Register Full Flag	
		MA1F	Match 1 Flag	
		MA2F	Match 2 Flag	
		OR	Receiver Overrun Flag	
		NF	Noise Flag	
		FE	Framing Error Flag	
		PF	Parity Error Flag	
		RXUF	Receiver Buffer Underflow Flag	
29	SCI2	TDRE	Transmit Data Register Empty Flag	
		TC	Transmission Complete	
		TXOF	Transmitter Buffer Overflow Flag	
		LBKDIF	LIN Break Detect Interrupt Flag	
		IDLE	Idle Line Flag	
		RXEDGIF	RXD2 Pin Active Edge	
			Interrupt Flag	
		RDRF	Receive Data Register Full Flag	
		MA1F	Match 1 Flag	
		MA2F	Match 2 Flag	
		OR	Receiver Overrun Flag	
		NF	Noise Flag	
		FE	Framing Error Flag	
		PF	Parity Error Flag	
		RXUF	Receiver Buffer Underflow Flag	
30	EPORT0	EPF0	Edge port 0 flag 0	Write EPF0 = 1
		EPF1	Edge port 0 flag 1	Write EPF1 = 1

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Source	Module	Flag	Source Description	Flag Clearing Mechanism
		EPF2	Edge port 0 flag 2	Write EPF2 = 1
		EPF3	Edge port 0 flag 3	Write EPF3 = 1
		EPF4	Edge port 0 flag 4	Write EPF4 = 1
		EPF5	Edge port 0 flag 5	Write EPF5 = 1
		EPF6	Edge port 0 flag 6	Write EPF6 = 1
		EPF7	Edge port 0 flag 7	Write EPF7 = 1
31	EPORT1	EPF0	Edge port 1 flag 0	Write EPF0 = 1
		EPF1	Edge port 1 flag 1	Write EPF1 = 1
		EPF2	Edge port 1 flag 2	Write EPF2 = 1
		EPF3	Edge port 1 flag 3	Write EPF3 = 1
		EPF4	Edge port 1 flag 4	Write EPF4 = 1
		EPF5	Edge port 1 flag 5	Write EPF5 = 1
		EPF6	Edge port 1 flag 6	Write EPF6 = 1
		EPF7	Edge port 1 flag 7	Write EPF7 = 1

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8. Embedded Programmable Timer (EPT)

8.1. Introduction

Embedded Programmable Timer(EPT) is a 24-bits timer that provides precise interrupts at regular intervals with minimal processor intervention. The timer can either count down from the reload value, or be a free-running down-counter.

EPT interrupt can trigger an exception(vector number = 24).

EPT module can be removed by clearing parameter “EPT” to 0 for reducing core gate count.

8.2. Memory Map and Registers

8.2.1. Memory Map

EPT base address is defined as EIC_BASEADDR + 0x1000. The default based address (EPT_BASEADDR) is 0xE000_1000. **Table 8-1** shows the offset address of EPT registers. EPT module occupies 4K address area.

Table 8-1: Programmable Timer Module Memory Map

Offset Address	Bits[31:0]	Access
0x0000_0000	EPT Control and Status Register (EPTCSR)	S/U
0x0000_0004	EPT Reload Register (EPTRLD)	S/U
0x0000_0008	EPT Count Register (EPTCNT)	S/U
0x0000_000C	Reserved	S/U

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8.2.2. Register Descriptions

This subsection contains a description of the EPT module registers.

8.2.2.1. EPT Control Status Register (EPTCSR)

Address: EPT_BASEADDR + 0x0000_0000

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							CNTFLAG
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0					CLKSRC	INTEN	CNTEN
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 8-1: EPT Control Status Register (EPTCSR)

CNTFLAG — Count Down to 0 flag

The read-only bit indicates timer counted to 0. It will be reset by HRESETn.

1 = The timer counted down to 0.

0 = The timer is still counting down.

CLKSRC — Count clock source select

The read/write bit is used to select the count clock source . It will be reset by HRESETn.

1 = Core clock.

0 = External reference clock.

INTEN — EPT Interrupt Request Enable

The read/write bit is used to enable EPT's interrupt when timer counted down to 0, It will be reset by RESET.

1 = EPT exception request occurs when timer counted down to 0.

0 = EPT exception request will not occur when timer counted down to 0.

CNTEN — Counter Enable

The read/write bit is used to enable EPT's counter. It will be reset by RESET.

1 = Counter is enabled

0 = Counter is disabled

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8.2.2.2. EPT Reload Register (EPTRLD)

Address: EPT _BASEADDR + 0x0000_0004

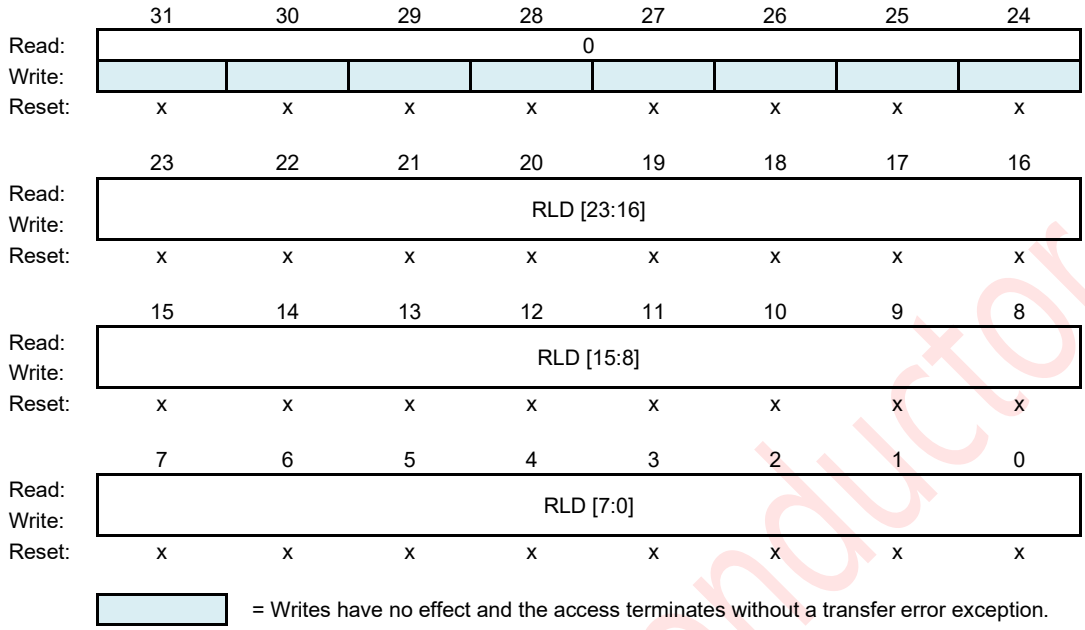


Figure 8-2: EPT Reload Register (EPTRLD)

RLD[23:0] — Reload Value

The read/write RLD[23:0] field specifies the reload value when timer counted down to 0 . The register has no reset value. The RLD value can be any value in the range 0x00000001 ~ 0x00FFFFFF. Value 0 has no effect. To generate a period timer with N clock cycles, set RLD to N-1.

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8.2.2.3. EPT Count Register (EPTCNT)

Address: EPT _BASEADDR + 0x0000_0008

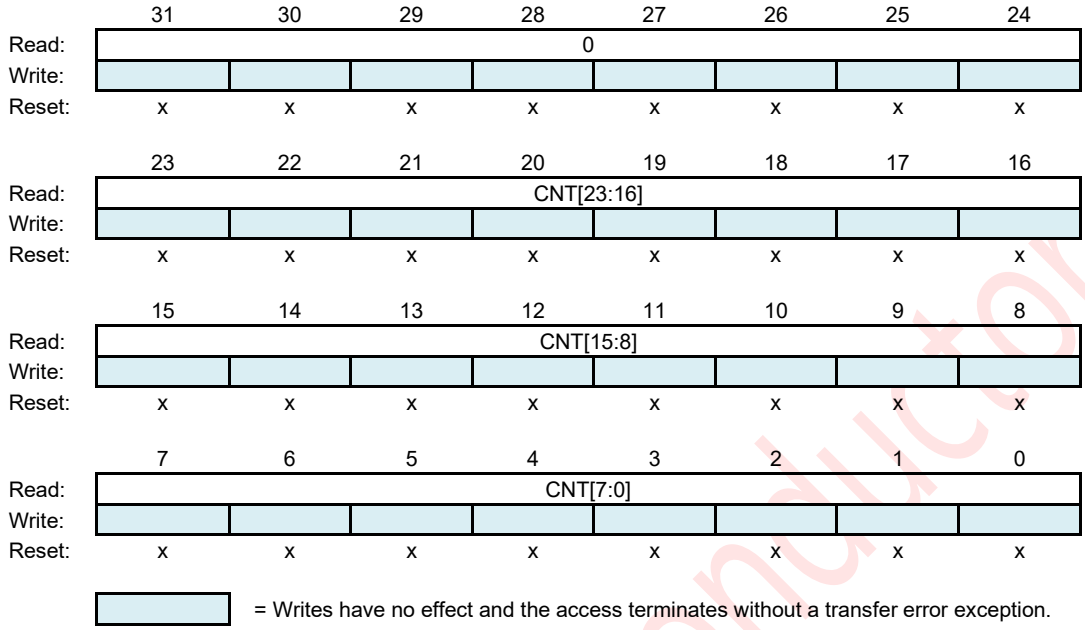


Figure 8-3: EPT Counter Register (EPTCNT)

CNT[23:0] — EPT Counter Value

The read-only register indicates the current count value of EPT timer. The register has no reset value.

Reads will return the current value of EPT counter. A write of any value to this register will clear the counter value to 0 and also the CNTFLAG to 0.

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8.3. Function Description

When Enabled, EPT counts down from the value set by RLD to zero, and wrap reloads the value in RLD on the next clock cycle, then down-counts by subsequent clock cycles, Writing zero to RLD disables the counter on next wrap. When EPT counts to zero, the CLFAG bit will be set to 1, and then the EPT will trigger the EPT interrupt if INTEN is enabled.

Reading CSR clears the CFLAG bit to 0. Writing any value to CNT also clears the CFLAG bit to 0.

8.3.1. Count Timing

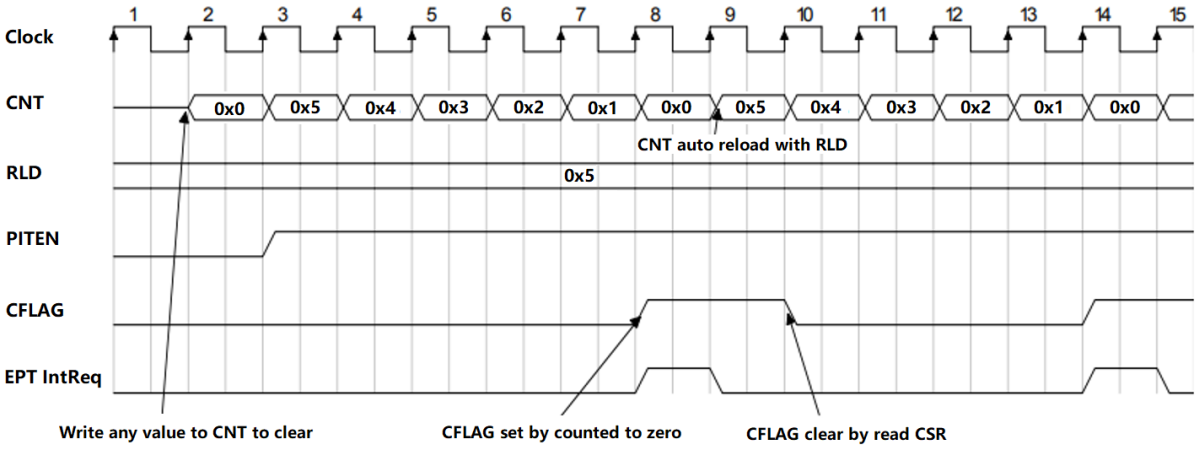


Figure 8-4: EPT Count Timing

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9. Clock and Power Control Module (CLKPWRM)

9.1. Overview

The Clock Module contains:

- PLL: Internal VCO PLL
- FXOSC: External Fast Speed Crystal Oscillator(12MHz)
- SIRC: Internal Low Speed 128Khz Oscillator
- SXOSC: External Low Speed Crystal Oscillator(32768Hz)
- Status and Control Registers
- Clock and Power Control Logic

9.2. Features

Features of the clock module include:

- Two System Clock Sources
  - Internal PLL Clock
  - External Fast Speed Crystal Oscillator(FXOSC)
- Individual Clock Divider for IPS, System and ADC Clock
- Support Low-power Mode
- Modules can be separately stopped by setting MSCR

9.3. Clock Structure

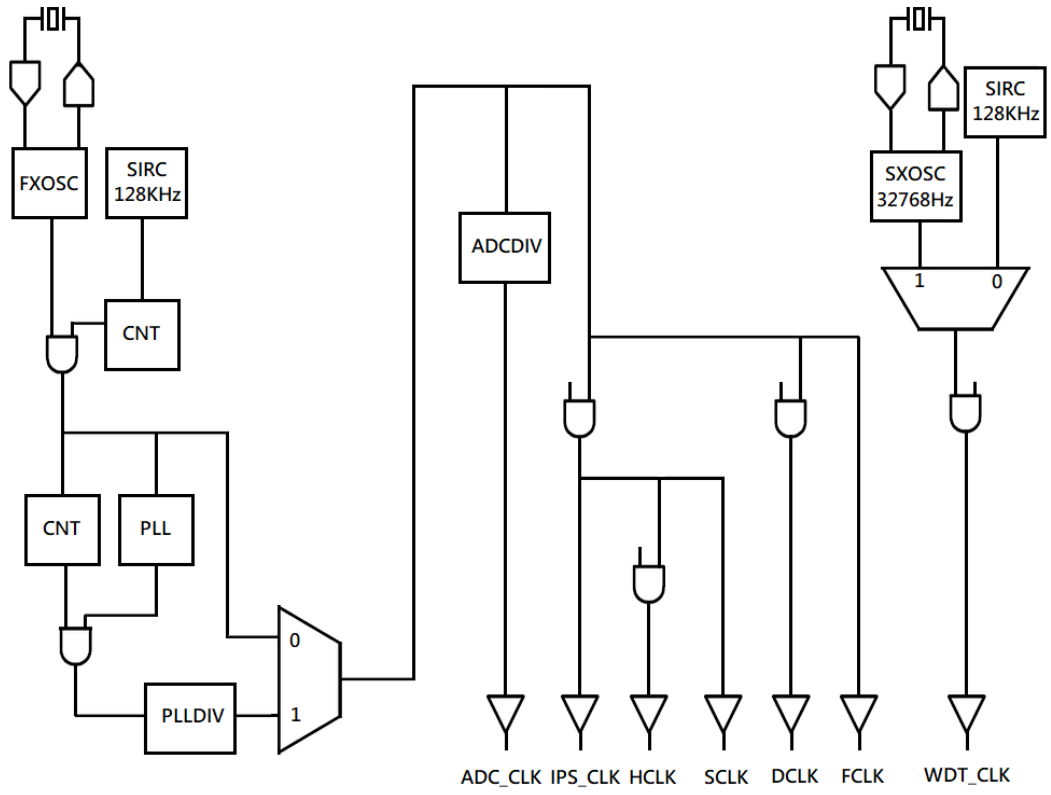


Figure 9-1: **Clock Structure**

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9.4. Clock Source Select

System Clock Source can be Internal PLL clock or external high speed crystal oscillator(FXOSC). Clock source Select is based on the PLLEN bit of SYNCR register. If the PLLEN bit is set then internal PLL is the system clock source, otherwise the system clock source is external high speed crystal oscillator(FXOSC).

9.4.1. Low-Power Options

9.4.1.1. Wait And Doze Modes

In wait and doze modes, the system clocks to the peripherals and Embedded-Flash are enabled, the clocks to the CPU, ROM, SRAM are stopped. Each module can disable the module clocks locally at the module level or by setting MSCR.

9.4.1.2. Stop Mode

In stop mode, all system clocks are disabled.
CAUTION: Do not program or erase EFLASH during stop mode.

9.5. Memory Map and Registers

The clock programming module consists of below registers:

- Synthesizer Control Register (SYNCR)
- Low Speed Oscillator Control Register (LOSCCR)
- PLL Configuration and Status Register(PLLCSR)
- Module stop control register (MSCR)
- EPT External Clock Source Enable Control Register(ECSECR)
- OSC Bist Test Configuration Register1(OBTCR1)
- OSC Bist Test Configuration Register2(OBTCR2)
- OSC Bist Test Control Register(OBTCTLR)
- OSC Bist Test Counter Register(OBTCNTR)
- OSC Bist Test Result Register(OBTRR)

This subsection describes the memory map and registers of the Clock Module. The Clock Module base address is 0x4003_0000. **Table 9-1** shows the offset address of Clock registers.

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9.5.1. Memory Map

Table 9-1: Clock Memory Map

Address	Bits[31:0]	Access[1]
0x0000	Synthesizer Control Register (SYNCR)	S
0x0004	Low Speed Oscillator Control Register (LOSCCR)	S
0x0008	PLL Configuration and Status Register(PLLCSR)	S
0x000C	Module Stop Control Register (MSCR)	S
0x0010	EPT External Clock Source Enable Control Register(ECSECR)	S
0x0014	OSC Bist Test Configuration Register1(OBTCR1)	S
0x0018	OSC Bist Test Configuration Register2(OBTCR2)	S
0x001C	OSC Bist Test Control Register(OBTCTLR)	S
0x0020	OSC BIST Test Counter Register(OBTCNTR)	S
0x0024	OSC BIST Test Result Register(OBTRR)	S

Note:

S = supervisor-only access. Accessing supervisor only address locations in user mode has no effect and result in a cycle termination transfer error.

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9.5.2. Register Description

This subsection provides a description of the clock module registers.

9.5.2.1. Synthesizer Control Register (SYNCR)

The synthesizer control register (SYNCR) is read/write always.

Address: CLOCK_BASEADDR + 0x0000_0000

	31	30	29	28	27	26	25	24
Read:	SYNCTEST[1:0]		SYSRAM3 LPEN	SYSRAM2 LPEN	SYSRAM1 LPEN	SYSRAM0 LPEN	PLLOCKM	ENLOWPO WER
Write:								
Reset:	0	0	0	0	0	0	0	1

	23	22	21	20	19	18	17	16
Read:	PLLDIV[5:0]						0	0
Write:								
Reset:	0	0	0	0	0	1	0	0

	15	14	13	12	11	10	9	8
Read:	ADCDIV[3:0]				LOSCEN	PLLSRCEN	PLLEN	SLEEP
Write:								
Reset:	0	0	1	0	1	1	0	0

	7	6	5	4	3	2	1	0
Read:	DISPLAYR AMLPEN	CLKOUTS EL	STBYMD[1:0]		CACHERA MLPEN	ADCEN	0	LOSCLPEN
Write:								
Reset:	1	0	1	1	1	1	0	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 9-2: Synthesizer Control Register (SYNCR)

SYNCTEST[1:0] — SYNCR Write Access Sequence In

The writable bits of SYNCR register can not be changed, unless the correct sequence is written. The right sequence is: 2'b01 → 2'b10 → 2'b11. After these two bits are written by this sequence, these two bits' value == 2'b11, then the writable bit of SYNCR register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

SYSRAM3LPEN — System RAM3(address range from 0x0083_0000 to 0x83_FFFF) Low Power Enable bit when the chip enters low power mode.

The low power mode of System RAM0 is achieved by switch-off the supply of the RAM and the content of the RAM will be lost.

1 = Low power mode of SYSRAM3 is enabled when the chip enters low power mode.

0 = Low power mode of SYSRAM3 is disabled when the chip enters low power mode.

SYSRAM2LPEN — System RAM2 (address range from 0x0082_0000 to 0x82_FFFF) Low Power Enable The low power mode of System RAM2 is achieved by switch-off the power supply to the RAM and the content of the RAM will be lost.

1 = Low power mode of SYSRAM2 is enabled when the chip enters low power mode.

0 = Low power mode of SYSRAM2 is disabled when the chip enters low power mode.

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SYSRAM1LPEN — System RAM1(address range from 0x0081_0000 to 0x81_FFFF) Low Power Enable
The low power mode of System RAM1 is achieved by switch-off the power supply to the RAM and the content of the RAM will be lost.

1 = Low power mode of SYSRAM1 is enabled when the chip enters low power mode.
0 = Low power mode of SYSRAM1 is disabled when the chip enters low power mode.

SYSRAM0LPEN — System RAM0(address range from 0x0080_0000 to 0x80_FFFF) Low Power Enable
The low power mode of System RAM0 is achieved by switch-off the power supply to the RAM and the content of the RAM will be lost.

1 = Low power mode of SYSRAM0 is enabled when the chip enters low power mode.
0 = Low power mode of SYSRAM0 is disabled when the chip enters low power mode.

PLLOCKM — PLL Lock detection flag which is generated by PLL macro.

1 = PLL Lock is generated by PLL macro when PLLEN is set.
0 = PLL Lock is not generated by PLL macro when PLLEN is set.

ENLOWPOWER — Enable Enter Low power mode status Bit

Before system enters standby mode, be sure that this bit is set, otherwise the low power mode will not be entered successfully. This bit is set after recovery from low power mode, and cleared by hardware when entering low power mode

1 = Enable Enter Low power mode status bit
0 = Low power mode is not allowed

PLLDIV[5:0] — PLL Clock Divider

This field sets the divider value for PLL clock. The default value is 6'b000001 (divide by two). See **Table 9-2** for other divider values.

Table 9-2: PLL Clock Divider

PLLDIV[5:0]	Divider Value
000000	Divide-by-2
000001	Divide-by-2
000010	Divide-by-4
000011	Divide-by-6
000100	Divide-by-8
000101	Divide-by-10
…..	…..
…..	…..
111111	Divide-by-126

Note: The frequency of the system clock should not be greater than 300MHz.

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ADCDIV[3:0] — ADC Clock Divider

This field sets the divider value for ADC clock. The default value is 4'b0000(divide by one). See **Table 9-3** for other divider values..

Table 9-3: ADC Clock Divider

ADCDIV[3:0]	Divider Value
0000	Divide-by-1
0001	Divide-by-2
0010	Divide-by-3
0011	Divide-by-4
0100	Divide-by-5
0101	Divide-by-6
0110	Divide-by-7
0111	Divide-by-8
1000	Divide-by-9
1001	Divide-by-10
1010	Divide-by-11
1011	Divide-by-12
1100	Divide-by-13
1101	Divide-by-14
1110	Divide-by-15
1111	Divide-by-16

LOSCEN — Internal Low Speed 128KHz Oscillator Enable Bit

1 = Internal Low Speed 128KHz Oscillator is enabled
0 = Internal Low Speed 128KHz Oscillator is disabled

PLLSRCEN — This bit determines whether system clock will be stopped or not when PLLEN is changed from 0 to 1.

1 = System clock will not be stopped and System clock source is from FXOSC until PLL locked
0 = System clock will be stopped until PLL locked

PLLEN — PLL Enabled control bit.

1 = PLL is enabled and the system clock source is PLL
0 = PLL is disabled and the system clock source is FXOSC

SLEEP — Chip Sleep Mode Control Bit

Set the SLEEP bit, the chip will enter standby mode indicated by STBYMD[1:0].
The operation is the same as "stop" instruction.

Note: SLEEP is valid only when STBYMD[1] = 1'b1. This is not the same case as the stop instruction because the stop instruction is always valid.

DISPLAYRAMLPEN — Display RAM (address range from 0x0084_0000 to 0x8b_ffff) Low Power Enable bit when the chip enters low power mode.

The low power mode of Display RAM is achieved by switch-off the power supply to the RAM and the content of the RAM will be lost.

1 = Low power mode of DISPLAYRAM is enabled when the chip enters low power mode.

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0 = Low power mode of DISPLAYRAM is disabled when the chip enters low power mode.

CLKOUTSEL — Clock Out Select Bit

Table 9-4: CLKOUTSEL Mode

CLKOUTSEL	CLKOUT
0	System clock
1	128KHz clock

STBYMD[1:0] — Sleep Operation Control Bits

STBYMD[1:0] control clock source, system clock operation and LDO State in sleep mode, as shown in **Table 9-5**.

Table 9-5: Sleep Operation Control Bit in Sleep Mode

STBYMD	ADC Clock	System Clocks	Clock Source	LDO
00	Enable	Disabled	Enable	Normal
01	Disabled	Disabled	Enable	Normal
10	Disabled	Disabled	Disabled	Normal
11	Disabled	Disabled	Disabled	Standby

CACHERAMLPEN — CACHE RAM Low Power Enable Bit.

This bit is enabled when the chip enters low power mode. The low power mode of CACHE RAM is achieved by switch-off the power supply to the RAM and the content of the RAM will be lost.

1 = Low power mode of CACHE RAM is enabled when the chip enters low power mode.

0 = Low power mode of CACHE RAM is disabled when the chip enters low power mode.

ADCEN — Analog-to-digital converter Clock Enable Bit

1 = ADC Clock is enable

0 = ADC Clock is disable

LOSCLPEN — Internal Low Speed 128KHz Oscillator Low Power Enable

If the LOSCLPE is set, the internal low speed 128KHz oscillator will be stopped during the standby mode.

1 = Low power mode of Internal Low Speed 128KHz Oscillator is enabled

0 = Low power mode of Internal Low Speed 128KHz Oscillator is disabled

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9.5.2.2. Low Speed Oscillator Control and Status Register (LOSCCSR)

Address: CLOCK_BASEADDR + 0x0000_0004

	31	30	29	28	27	26	25	24
Read:	LOSCCSTEST[1:0]		0	SIRCST[4:0]				
Write:								
Reset:	0	0	0	1	1	1	1	1

	23	22	21	20	19	18	17	16
Read:	SXOSCST[15:8]							
Write:								
Reset:	0	1	0	1	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	SXOSCST[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	SIRCRDY	SXOSCRDY	WDTCLKCHGDONE	0			WDTCLKSEL	SXOSCEN
Write:								
Reset:	1	1	1	0	0	0	0	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 9-3: Low Speed Oscillator Control and Status Register (LOSCCSR)

LOSCCSTEST[1:0] — LOSCCSR Write Access Sequence In

The writable bit of IOSCCSR register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by the sequence, these two bits' value == 2'b11, then the writable bit of LOSCCSR register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

SIRCST[4:0] — Internal Low Speed Oscillator Stable Time Value

The internal low speed oscillator(SIRC) will wait SIRCST[4:0] cycles of 32KHz (SIRC divided by 4) oscillator, and then be ready for output clock after switching on.

SXOSCST[15:0] — External Low Speed Oscillator Stable Time Value

The external low speed oscillator(SXOSC) will wait SXOSCST[15:0] cycles of 128KHz(source of SIRC) oscillator, and then be ready for output clock after switching on.

SIRCRDY — Internal low speed oscillator (SIRC) ready flag.

1 = Internal low speed oscillator (SIRC) is ready

0 = Internal low speed oscillator (SIRC) is not ready

SXOSCRDY — External low speed oscillator (SXOSC).

1 = External low speed oscillator (SXOSC) is ready

0 = External low speed oscillator (SXOSC) is not ready

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WDTCLKCHGDONE — WDT clock switch done flag.

This bit will be changed to low when WDTCLKSEL is changed. When WDTCLK change is done, then this bit will be set.

1 = WDT clock switch done and WDT can work normally

0 = WDT clock is switching and WDT can not be work normally

WDTCLKSEL — WDT clock selection control bit.

When changing WDT clock source from SXOSC to SIRC, the WDTCLKSEL bit should be cleared before turning off SXOSC.

1 = WDT clock source is SXOSC(32.768KHz)

0 = WDT clock source is SIRC 128Khz

SXOSCEN — SXOSC Enable Setting

1 = SXOSC is enabled for WDT application.

0 = SXOSC crystal is disabled for WDT application., In addition, WDTCLKSEL should be cleared now, otherwise WDT clock will be lost.

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9.5.2.3. PLL Configuration And Status Register (PLLCSR)

Address: CLOCK_BASEADDR + 0x0000_0008

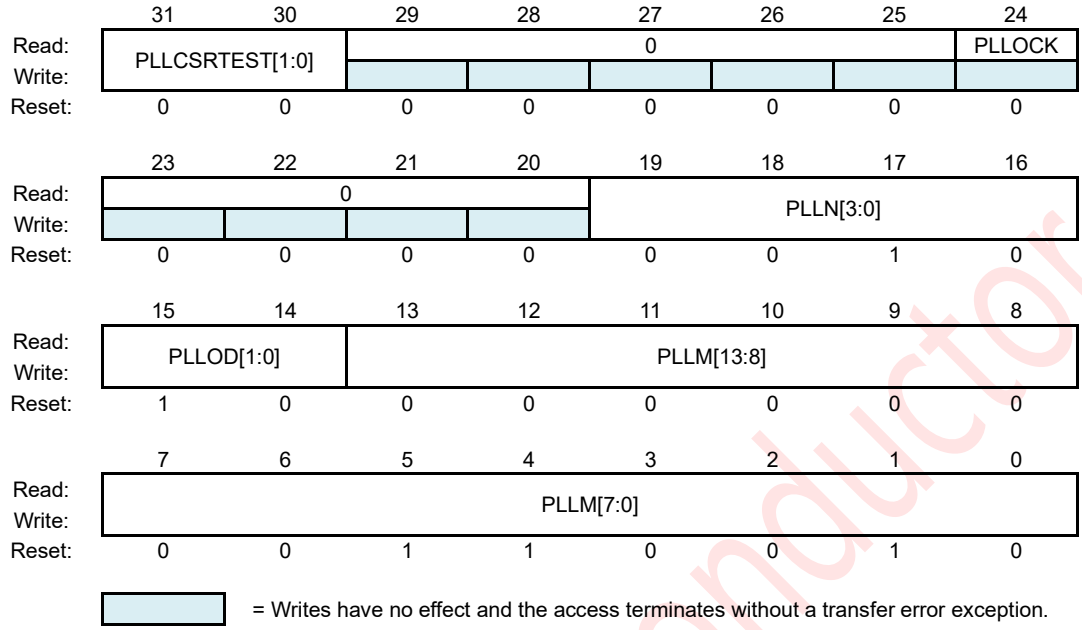


Figure 9-4: PLL Configuration and Status Register (PLLCSR)

$$\text{PLL Output Frequency} = XIN \times \frac{M}{N} \times \frac{1}{NO}$$

PLLCSRTEST[1:0] — PLLCSR Write Access Sequence In

The writable bit of PLLCSR register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of PLLCSR register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

CAUTION: Please keep these conditions during usage:

1. 1MHz <= XIN/N <= 50MHz
2. 200MHz <= XIN*M/N <= 400MHz
3. M≥4
4. N≥1

PLLOCK — PLL Lock Flag

Once PLL is enabled, PLLOCK will be set after waiting for the number of cycles set in PLLOCKCR[PLLST].

1 = PLL is locked

0 = PLL is not locked

PLLN[3:0] — Input 4-bits divider control bits

This field sets the input divider value for PLL clock. The default value is 4'b0000. See **Table 9-6** for the available divider values.

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Table 9-6: PLL Input Divider

PLLN[3:0]	N
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

PLLOD[1:0] — Output divider control bits

This field sets the output divider value for PLL VCO clock. The default value is 2'b00. See **Table 9-7** for the available divider values.

Table 9-7: PLL VCO Output Clock Divider

PLLOD[1:0]	NO
00	Divide-by-1
01	Divide-by-2
10	Divide-by-4
11	Divide-by-8

PLLM[13:0] — Feedback 14-bits divider control bits

This field sets the PLL feedback divider value . The default value is 14'b0. See **Table 9-8** for the available divider values.

Table 9-8: PLL Feedback Divider Value

PLLM[13:0]	M
14'b00_0000_0000_0000	0
14'b00_0000_0000_0001	1
14'b00_0000_0000_0010	2
14'b00_0000_0000_0011	3
14'b00_0000_0000_0100	4
14'b00_0000_0000_0101	5

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PLLM[13:0]	M
…..	…..
…..	…..
14'b11_1111_1111_1111	16383

9.5.2.4. Module Stop Control Register (MSCR)

The Module Stop Control Register(MSCR) is read/write always.

Address: CLOCK_BASEADDR + 0x0000_000C

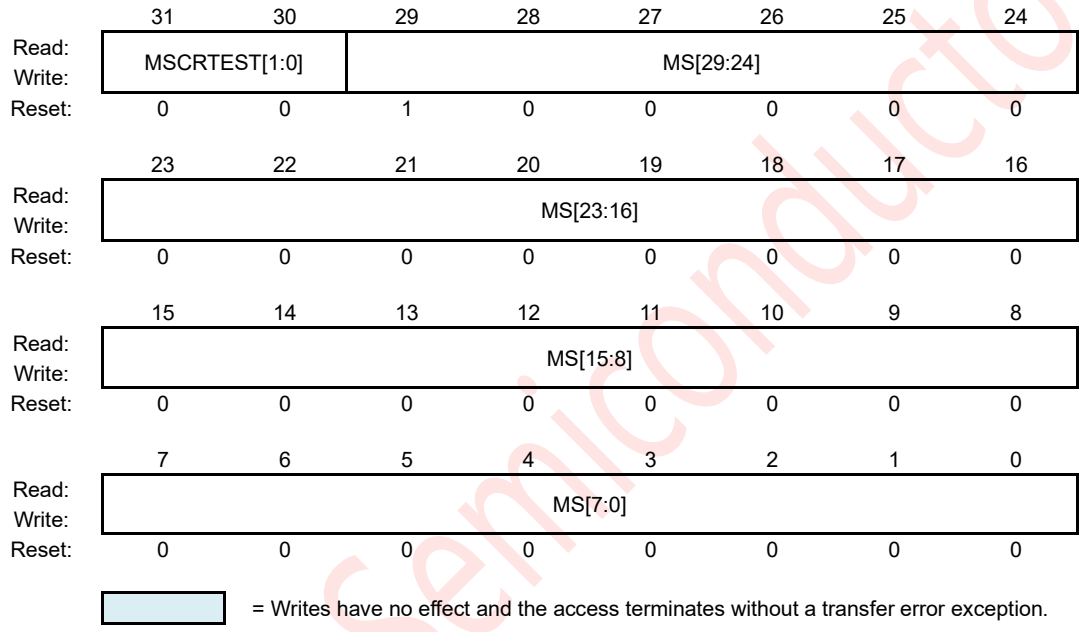


Figure 9-5: Module Stop Control Register (MSCR)

MSCRTEST[1:0] — MSCR Write Access Sequence In

The writable bit of MSCR register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of MSCR register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

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MS[29:0] — Module Stop Bits

The MS[25:0] bits disable the modules' clocks in the top level. (refer to **Table 9-9** MS[29:0] Bits Corresponding Modules).

1 = Module Clock is disabled

0 = Module Clock is enabled

Table 9-9: **MS[29:0] Bits Corresponding Modules**

MS Bit	Corresponding Module
0	Blender
1	COMP0
2	COMP1
3	ADC
4	PIT0
5	PIT1
6	PIT2
7	PIT3
8	RTC
9	DMA
10	PWM0
11	PWM1
12	EPORT0
13	EPORT1
14	XBAR
15	OPTION
16	RESET
17	WDT
18	SCI0
19	CCM
20	I2C
21	SCI1
22	SCI2
23	CAN
24	EPORT2
25	QSPI0
26	QSPI1
27	QSPI2
28	RGB
29	USBC

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9.5.2.5. EPT External Clock Source Enable Control Register (ECSECR)

Address: CLOCK_BASEADDR + 0x0000_0010

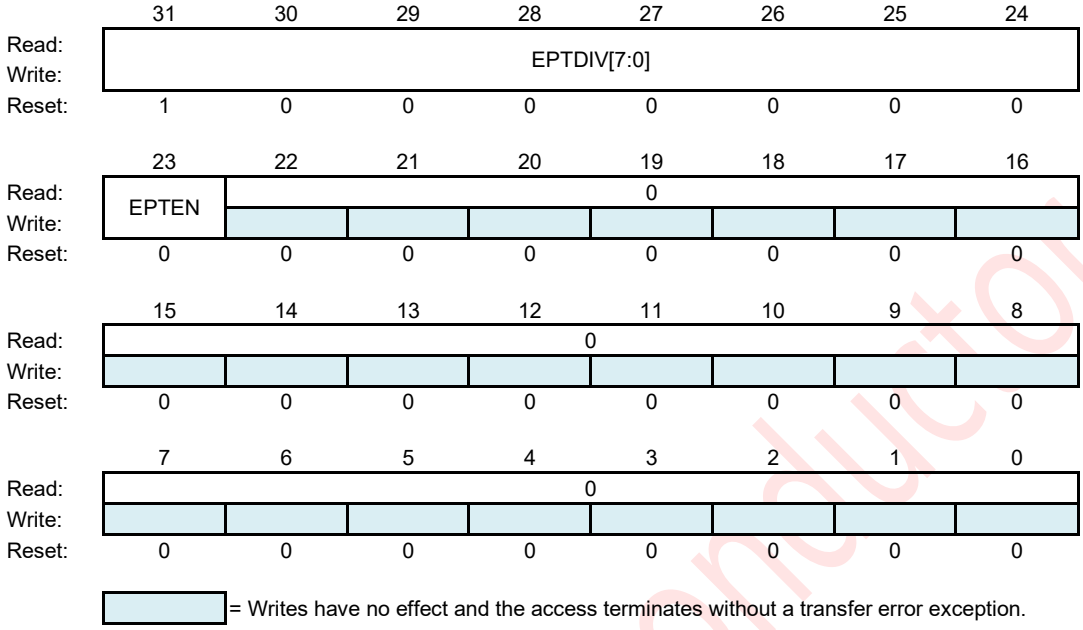


Figure 9-6: EPT External Clock Source Enable Control Register (ECSECR)

EPTDIV[7:0] — EPT Clock Divider

This field sets the divider value for EPT clock. The default value is 8'h80. See **Table 9-10** for other available divider values.

Table 9-10: EPT Clock Divider

EPTDIV[7:0]	Divider Value
00000000	Divide-by-1
00000001	Divide-by-2
00000010	Divide-by-3
00000011	Divide-by-4
00000100	Divide-by-5
00000101	Divide-by-6
…..	…..
…..	…..
11111110	Divide-by-255
11111111	Divide-by-256

EPTEN — EPT Clock Enable Bit

If the EPTEN bit is set, EPT clock will be divided from system clock.

1 = EPT clock is enable

0 = EPT clock is disable

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9.5.2.6. OSC Bist Test Configuration Register1 (OBTCR1)

Address: CLOCK_BASEADDR + 0x0000_0014

	31	30	29	28	27	26	25	24
Read: Write:	BIST_HOLD_TARGET[15:8]							
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read: Write:	BIST_HOLD_TARGET[7:0]							
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read: Write:	BIST_TARGET[15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	BIST_TARGET[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 9-7: OSC Bist Test Configuration Register1 (OBTCR1)

BIST_HOLD_TARGET[15:0] — Bist clk hold count target value
These bits set the the amount of wait clk under test stable after the trim value is changed.

BIST_TARGET[15:0] — Bist clk count target value.

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9.5.2.7. OSC Bist Test Configuration Register2 (OBTCR2)

Address: CLOCK_BASEADDR + 0x0000_0018

	31	30	29	28	27	26	25	24
Read: Write:	BIST_TEST_TARGET[15:8]							
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read: Write:	BIST_TEST_TARGET[7:0]							
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read: Write:	BIST_TEST_CTRIM_MARGIN[15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	BIST_TEST_CTRIM_MARGIN[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 9-8: OSC Bist Test Configuration Register2 (OBTCR2)

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BIST_TEST_TARGET[15:0] — Reserved. Not available to users.

BIST_TEST_CTRIM_MARGIN[15:0] — Reserved. Not available to users.

9.5.2.8. OSC Bist Test Control Register (OBTCTLR)

Address: CLOCK_BASEADDR+0x0000_001C

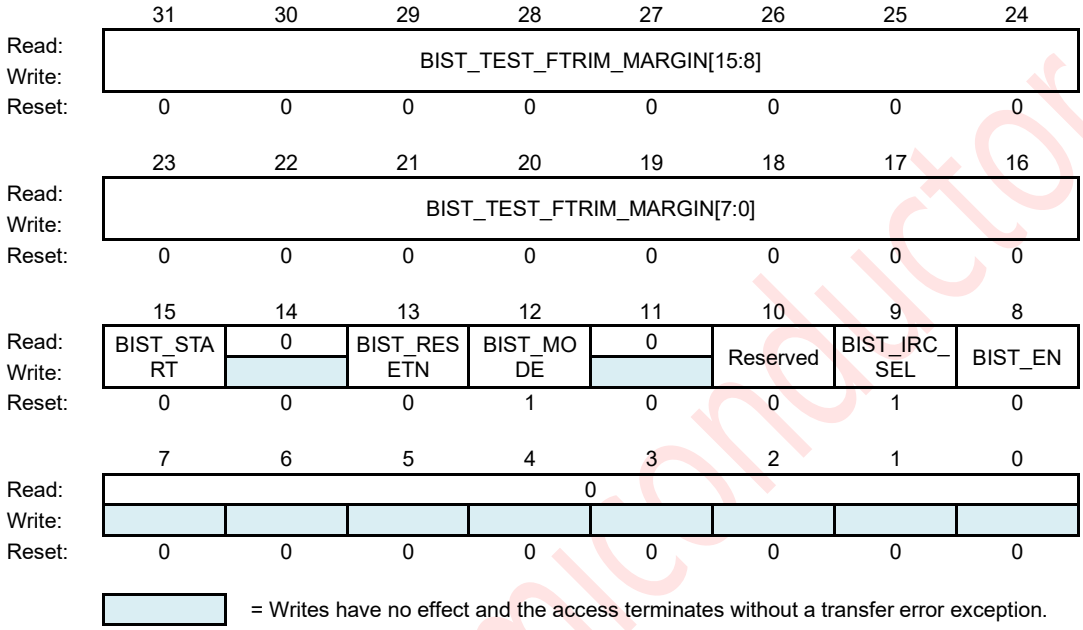


Figure 9-9: OSC Bist Test Control Register (OBTCTLR)

BIST_TEST_FTRIM_MARGIN[15:0] — Reserved. Not available to users.

BIST_START — Bist Start

1 = start
0 = stop

BIST_RESETN — Bist Reset Negate

1 = Negate Bist Reset
0 = Assert Bist Reset

BIST_MODE — Bist Mode

1 = trace mode(for measure the frequency of PLL or 128K clock)
0 = trim mode

Note: Only trace mode is implemented on this chip.

BIST_IRC_SEL — PLL or 128KHz clock selection

1 = PLL Clock is selected
0 = 128K Clock is selected

BIST_EN — Reference Clock Enable

1 = enable
0 = disable

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9.5.2.9. OSC BIST Test Counter Register (OBTCNTR)

Address: CLOCK_BASEADDR+0x0000_0020

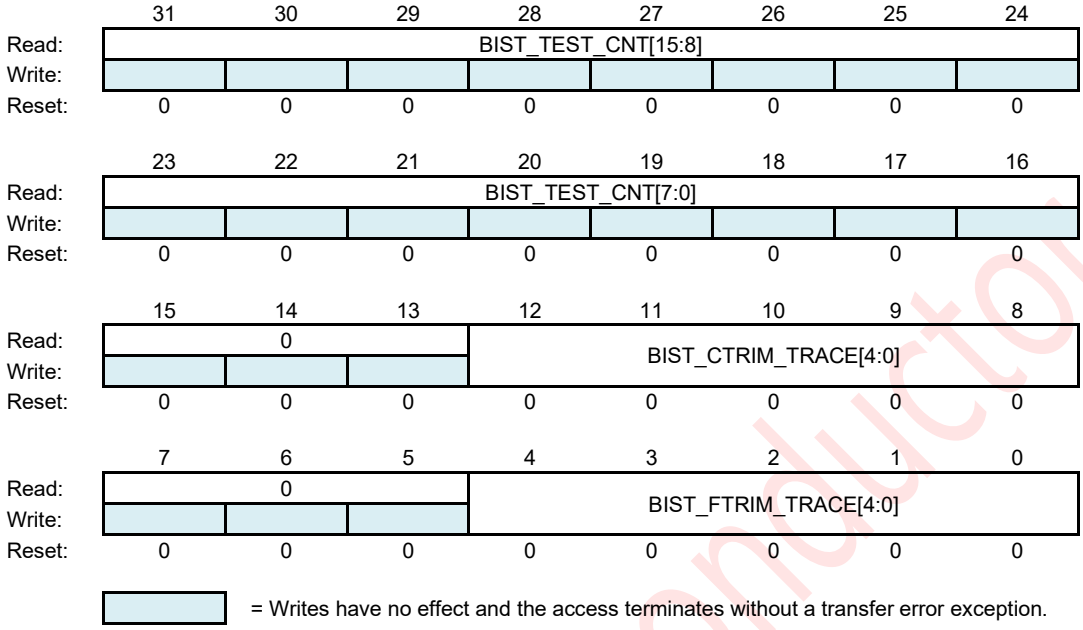


Figure 9-10: OSC BIST Test Counter Register (OBTCNTR)

BIST_TEST_CNT[15:0] — Bist Test Counter Value

BIST_CTRIM_TRACE[4:0] — Bist Ctrim Trace Value

BIST_FTRIM_TRACE[4:0] — Bist Ftrim Trace Value

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9.5.2.10. OSC BIST Test Result Register (OBTRR)

Address: CLOCK_BASEADDR+0x0000_0024

	31	30	29	28	27	26	25	24
Read:	0						BIST_DONE	BIST_PASS
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							BISTRE-SULT[16]
Write:								
Reset:	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8
Read:	BISTRESULT[15:8]							
Write:								
Reset:	1	0	0	0	0	1	1	1

	7	6	5	4	3	2	1	0
Read:	BISTRESULT[7:0]							
Write:								
Reset:	0	1	1	1	1	0	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 9-11: OSC BIST Test Result Register (OBTRR)

BIST_DONE — Bist Done

1 = done

0 = not done

BIST_PASS — Bist Pass

1 = PASS

0 = FAIL

BISTRESULT[16:0] — Bist Trim Result

VALID WHEN bist_done = 1 & bist_pass = 1

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9.6. Functional Description

9.6.1. Turning on PLL

The following steps are suggested:

1. Configuring SYNCR[PLLSRCEN] first.
2. Configuring PLLCSR[PLLOD]/PLLCSR[PLLN]/PLLCSR[PLLM] according to the target VCO frequency.
3. Configuring SYNCR[PLLEN] and open PLL.
4. Waiting for SYNCR[PLLOCK] status and system clock will be changed to PLL clock.
5. Configuring SYNCR[PLLDIV] according to the target system frequency.

9.6.2. The Frequency of PLL Measurement

The following steps are suggested:

1. Setting BIST_RESETN bit to 0 for assert reset.
2. Setting BIST_TARGET counter value.
3. Setting BIST_MODE bit to 1.
4. Setting IRC_BIST_SEL bit to 1 for PLL measurement.
5. Setting BIST _START bit to 1.
6. Setting BIST_RESETN bit to 1 for negated reset.
7. Waiting for BIST_DONE bit.
8. Reading BIST_TEST_CNT for measuring the frequency of PLL clock.
9. Calculating the frequency of PLL clock according to BIST_TEST_CNT and the frequency of fxosc clock.

The Frequency of PLL clock is calculated as follow:

$$f_{PLL} = f_{fxosc} * BIST_TEST_CNT[15:0] / BIST_TARGET[15:0]$$

9.6.3. The Frequency of 128KHz Measurement

The following steps are suggested:

1. Setting BIST_RESETN bit to 0 for assert reset.
2. Setting BIST_TARGET counter value.
3. Setting BIST_MODE bit to 1.
4. Setting IRC_BIST_SEL bit to 0 for 128KHz clock measurement.
5. Setting BIST _START bit to 1.
6. Setting BIST_RESETN bit to 1 for negated reset.
7. Waiting for BIST_DONE bit.
8. Reading BIST_TEST_CNT for measuring the frequency of 128KHz clock.
9. Calculating the frequency of 128KHz clock according to BIST_TEST_CNT and the frequency of fxosc clock.

The Frequency of 128KHz is calculated as follow:

$$f_{128khz} = f_{fxosc} * BIST_TEST_CNT[15:0] / BIST_TARGET[15:0]$$

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10. Reset Control Module (RCM)

10.1. Overview

Reset Control Module is provided to determine the cause of reset, assert the appropriate reset signals to the system, and then to keep a history of reset causes.

10.2. Features

Module features include:

- Five Sources of Reset:
  - Power on Reset
  - External Reset Pin (RESET#)
  - Software Reset
  - Watchdog Timer Reset
  - Programmable Voltage Detect Reset
- Software-readable status flags indicating the cause of the last reset

10.3. Block Diagram

Figure 10-1 illustrates the reset controller

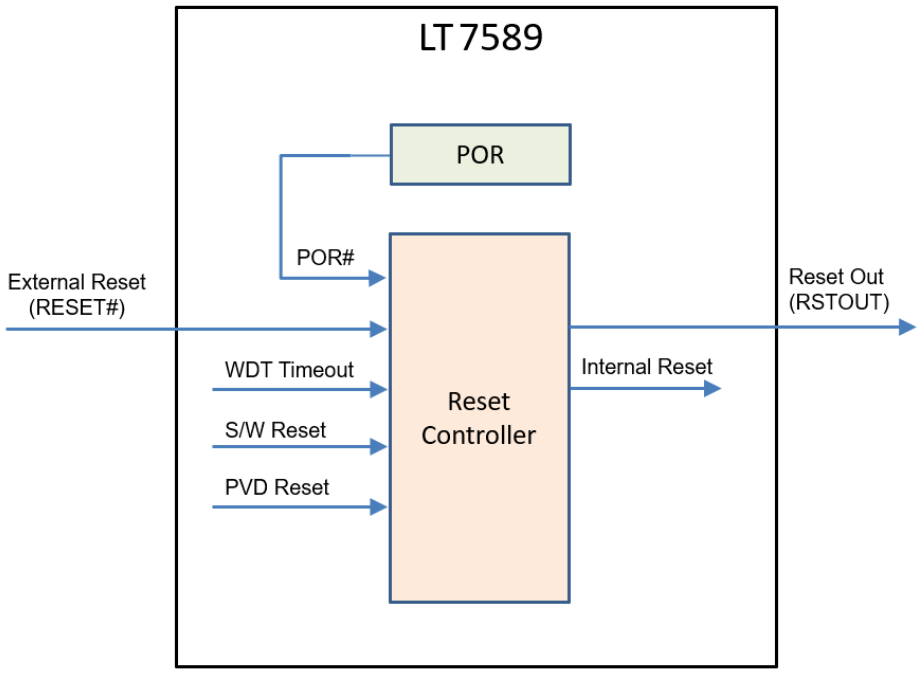


Figure 10-1: Reset Controller Block Diagram

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10.4. Memory Map and Registers

10.4.1. Memory Map

The reset controller programming model consists of these registers:

- •Reset Control Register (RCR) — Selects reset controller functions
- •Reset Status Register (RSR) — Reflects the state of the last reset source

This subsection describes the memory map and registers of Reset Controller Module. The Reset Controller base address is 0x4002_0000. See **Table 10-1** for the address map and the following paragraphs for a description of the registers.

Table 10-1: Reset Controller Address Map

Address	Bits[7:0]	Access 1
0x0000	Reserved	S/U
0x0001	RTR—Reset Test Register	S/U
0x0002	RSR—Reset Status Register	S/U
0x0003	RCR—Reset Control Register	S/U

Note: S/U = Supervisor or user mode access.

10.4.2. Register Description

10.4.2.1. Reset Test Register (RTR)

The Reset Test Register(RTR) is only for factory testing.

Address: RCM_BASEADDR+0x0000_0001

	7	6	5	4	3	2	1	0
Read:	TEST[1:0]		0	0	0	0	0	FPOR
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 10-2: Reset Test Register (RTR)

TEST[1:0] — RTR Write Access Sequence In

The writable bit of FPOR register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01->2'b10->2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of FPOR bit can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

FPOR — Force Power On Reset

Writing 0x5B to the RTR register, and then setting this bit will result in system power on reset.

The reset will result in the chip trimming again.

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10.4.2.2. Reset Status Register (RSR)

The Reset Status Register(RSR) contains a status bit for every reset source. When reset is entered, the cause of the reset condition is latched along with a value of 0 for the other reset sources that were not pending at the time of the reset condition. These values are then reflected in RSR. One or more status bits may be set at the same time. The cause of any subsequent reset is also recorded in the register, overwriting status from the previous reset condition.

RSR can be read at any time. Writing to RSR has no effect.

Address: RCM_BASEADDR+0x0000_0002

	7	6	5	4	3	2	1	0
Read:	ERST	PVD	SOFT	WDTR	POR	0	0	0
Write:								
Reset:	0	Reset Dependent						

= Writes have no effect and the access terminates without a transfer error exception.

Figure 10-3: Reset Status Register (RSR)

ERST — External Reset

This bit indicates that the last reset state was caused by an external reset.

1 = Last reset state was caused by an external reset

0 = Last reset state was not caused by an external reset

PVD — Programmable Voltage Detect

This bit indicates that the last reset state was caused by a PVD reset.

1 = Last reset state was caused by a PVD reset

0 = Last reset state was not caused by a PVD reset

SOFT — Software Reset Flag

This bit indicates that the last reset state was caused by software.

1 = Last reset state was caused by software.

0 = Last reset state was not caused by software.

WDTR — Watchdog Timer Reset Flag

This bit indicates that the last reset state was caused by a watchdog timer timeout.

1 = Last reset state was caused by a watchdog timer timeout.

0 = Last reset state was not caused by a watchdog timer timeout.

POR — Power-On Reset Flag

This bit indicates that the last reset state was caused by power-on reset.

1 = Last reset state was caused by power-on reset.

0 = Last reset state was not caused by power-on reset.

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10.4.2.3. Reset Control Register (RCR)

The Reset Control Register (RCR) allows software control for requesting a reset.

Address: RCM_BASEADDR+0x0000_0003

	7	6	5	4	3	2	1	0
Read:	0	0	0	0	0	0	0	FRCRSTOUT
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 10-4: Reset Control Register (RCR)

FRCRSTOUT — Force RSTOUT Pin

The FRCRSTOUT bit allows software to drive the external RSTOUT pin to Low or High State.

1 = Assert RSTOUT pin. Writing “1” to this bit will drive RSTOUT pin to Low.

0 = Negate RSTOUT pin. Writing “0” to this bit will drive RSTOUT pin to High.

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10.5. Functional Description

10.5.1. Reset Sources

Table 10-2 defines the sources of reset and the signals driven by the reset controller.

Table 10-2: Reset Source Summary

Source	Type
POR	Asynchronous
ERST	Asynchronous
Watchdog timer	Asynchronous
Software	Synchronous
PVD	Asynchronous

To protect data integrity, a synchronous reset source is not acted upon by the reset control logic until the end of the current bus cycle. Reset is then asserted on the next rising edge of the system clock after the cycle is terminated. Whenever the reset control logic must synchronize reset to the end of the bus cycle, and the internal bus monitor is automatically enabled.

Asynchronous reset sources usually indicate a catastrophic failure. Therefore, the reset control logic does not wait for the current bus cycle to complete. Reset is asserted immediately to the system.

10.5.1.1. Power-On Reset (POR)

At power up, the Reset Controller asserts system reset. System reset continues to be asserted until POR has reached a minimum acceptable level.

10.5.1.2. Watchdog Timer Reset

A watchdog timer timeout causes timer reset request to be recognized and latched.

10.5.1.3. Software Reset

If the SYSRESTEQ bit in 32-bits RISC Embedded Interrupt Controller (EIC) is set, the software reset will be generated. The reset controller asserts system reset for approximately 2048 cycles. Then the chip exits reset and resumes operation.

10.5.1.4. Programmable Voltage Detect Reset

When the PVDRE bit of the CCR register in Embedded Flash Module (EFM) is set, PVD will generate reset when the VDD exceeds the PVD threshold.

10.5.2. Reset Control Flow

The reset logic control flow is shown in **Figure 10-5**. All cycle counts given are approximate.

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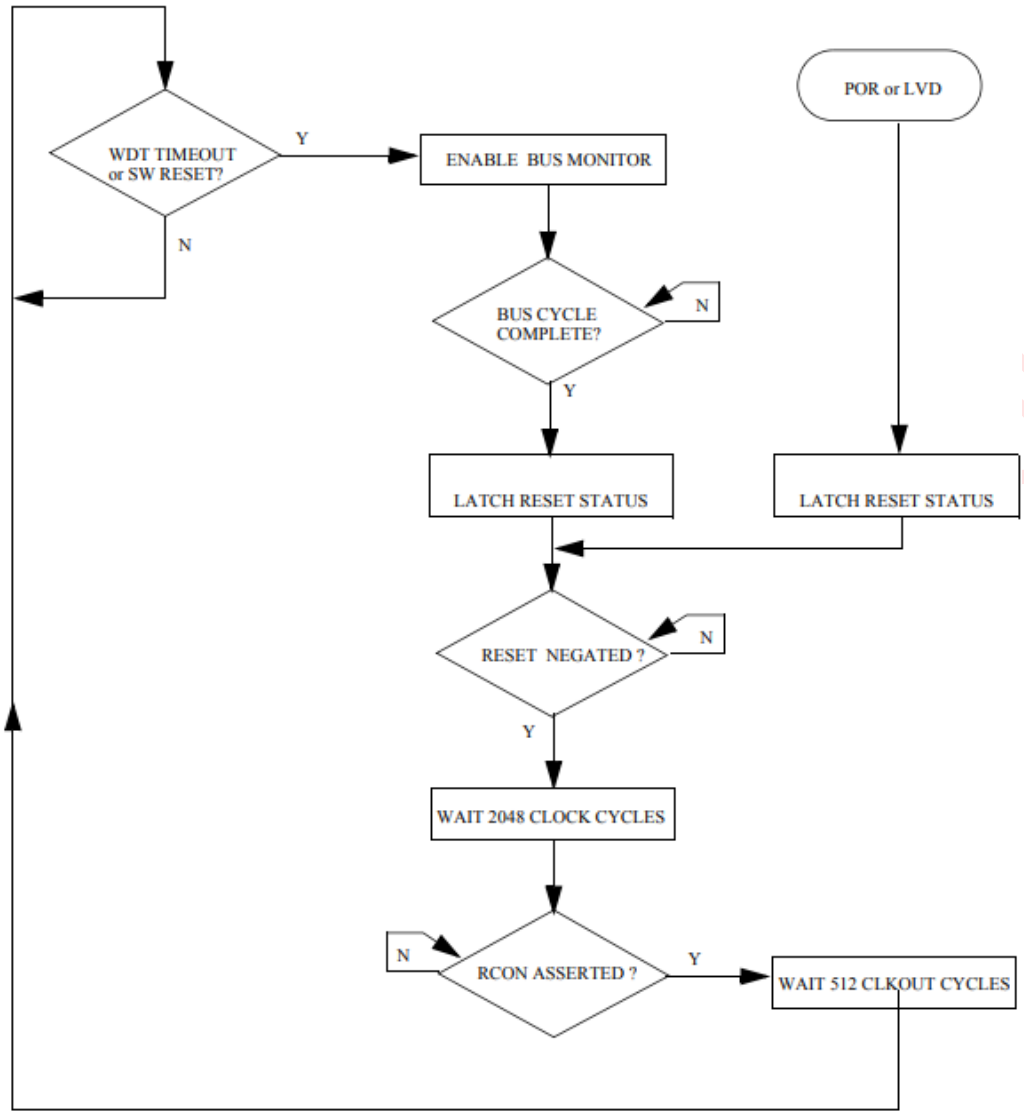


Figure 10-5: Reset Control Flow

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11. Static Random Access Memory (SRAM)

11.1. Introduction

The features of the LT7589's Static Random Access Memory (SRAM) include:

- On-chip 64K Bytes SRAM
- Fixed Address Space
- Byte, Half-word (16-bits), or Word (32-bits) Read/Write Accesses
- One Clock Per access (including bytes, Half-words, and Words)
- Supervisor or User Mode Access

11.2. Modes Of Operation

Access to the SRAM is not restricted in any way. The array can be accessed in supervisor and user modes.

11.3. Low-Power Modes

In wait, doze and stop mode, clocks to the SRAM are disabled. No recovery time is required when exiting these modes.

11.4. Reset Operation

The SRAM contents are undefined immediately following a power-on reset. SRAM contents are unaffected by system reset. If a synchronous reset occurs during a read or write access, then the access completes normally and any pipelined access in progress is stopped without corruption of the SRAM contents.

11.5. Interrupts

The SRAM module does not generate interrupt requests.

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12. Cache Module (CACHEM)

12.1. Introduction

Cache Module provides the processor with tightly-coupled processor-local memories and bus paths to EBI and QSPI0/1/2 memory spaces.

A cache is a block of high-speed memory locations containing address information (commonly known as a tag) and the associated data. The purpose is to reduce the average time of a memory access. Caches operate on two principles of locality:

- Spatial locality — An access to one location is likely to be followed by accessing to the adjacent locations (for example, sequential instruction execution or the utilization of a data structure).
- Temporal locality — An access to an area of memory is likely to be repeated within a short period of time (for example, execution of a code loop).

To minimize the quantity of control information stored, the spatial locality property is used to group several locations together under the same tag. This logical block is commonly known as a cache line.

When data are loaded into a cache, the access time for subsequent loads and stores are reduced. This will enhance overall performance. An access to information already in a cache is known as a cache hit, and other accesses are called cache misses.

Normally, caches are self-managing, with the updates occurring automatically. Whenever the processor wants to access a cacheable location, the cache hit is checked. If the access is a cache hit, the access occurs immediately. Otherwise, a location is allocated and the cache line is loaded from memory. Different cache topologies and access policies are possible.

However, they must comply with the memory coherency model of the underlying architecture. Caches introduce a number of potential problems, mainly because of:

- Memory accesses occurring at times other than when the programmer would normally expect them;
- The existence of multiple physical locations where a data item can be held.

The Cache Controller is targeted for use with any 32-bits AHB-bus based application that desires a cache function. This cache function can enhance performance by providing fast access to recently used code or data.

The local memory controller supports three operation modes:

1. Write-through — access to address spaces with this cache mode is cacheable.
   - A write-through read miss on the input bus causes a line read on the output bus of a 16-byte-aligned memory address containing the desired address. This miss data is loaded into the cache and is marked as valid and not modified.
   - A write-through read hit to a valid cache location returns data from the cache with no output bus access.
   - A write-through write miss bypasses the cache and writes to the output bus (no allocate on write miss policy for write-through mode spaces).
   - A write-through write hit updates the cache hit data and writes to the output bus.
2. Write-back — access to address spaces with this cache mode is cacheable.
   - A write-back read miss on the input bus will cause a line read on the output bus of a 16-byte-aligned memory address containing the desired address. This miss data is loaded into the cache and marked as valid and not modified.
   - A write-back read hit to a valid cache location will return data from the cache with no output bus access.

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- A write-back write miss will do a "read-to-write" (allocate on write miss policy for write-back mode spaces). A line read on the output bus of a 16 byte aligned memory address containing the desired write address is performed. This miss data is loaded into the cache and marked as valid and modified; and the write data will then update the appropriate cache data locations.

3. Non-cacheable — access to address spaces with this cache mode is not cacheable.

- These accesses bypass the cache and access the output bus.

The Cache Controller has two AHB-bus interfaces, a master, and a slave interface. The master interface has decode logic to determine the cache mode of valid address phase accesses. Master accesses will then access or bypass the cache depending on their cache mode. The slave interface is used for cache misses as well as accesses that bypass the cache.

The Cache Controller has a 2-way set-associative organization. The cache has 32-bits wide address and data paths, and a 16-byte line size. The cache tags and data storage use single port, synchronous RAMs. The Controller has a variety of read and write data buffers to improve performance. Cache misses and line pushes generate 4-beat 32-bits wrapping burst accesses with the critical word accessed first for maximum performance.

12.2. Block Diagram

These Cache module provides zero wait state access to RAM and cacheable address spaces.

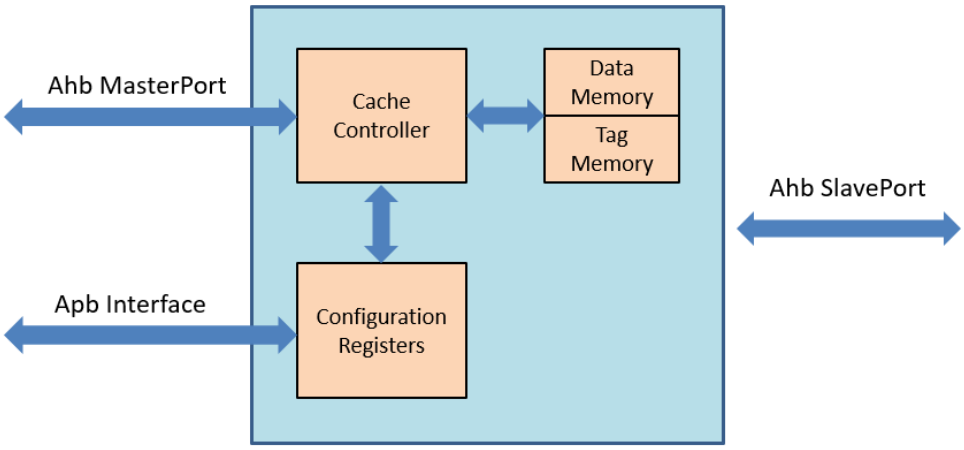


Figure 12-1: Cache Module Block Diagram

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12.3. Memory Map and Registers

12.3.1. Memory Map

This subsection describes the Cache Module memory map and registers. The Cache Module base address is 0x4019_0000. **Table 12-1** shows the offset address of these registers.

Table 12-1: Cache Module Memory Map

Address Offset	Bits[31:0]	Access
0x0000	Cache Control Register (LMEM_CCR)	S/U
0x0004	Cache Line Control Register (LMEM_CLCR)	S/U
0x0008	Cache Search Address Register (LMEM_CSAR)	S/U
0x000C	Cache Read/Write Value Register (LMEM_CCVR)	S/U
0x0020	Cache Access Register(LMEM_ACR)	S/U
0x0180	Cache Page Invalidation Start Address	S/U
0x0184	Cache Page Invalidate Size	S/U
0x0188	Cache Clock Gate	S/U

Notes:

1. S = CPU supervisor mode access only, U = CPU user mode access only
2. Accessing to supervisor-only address locations in user mode has no effect and result in a cycle termination transfer error

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12.3.2. Register Description

This subsection provides a description of the Cache module.

12.3.2.1. Cache Control Register (LMEM_CCR)

Address: CACHE_BASEADDR+0x0000_0000

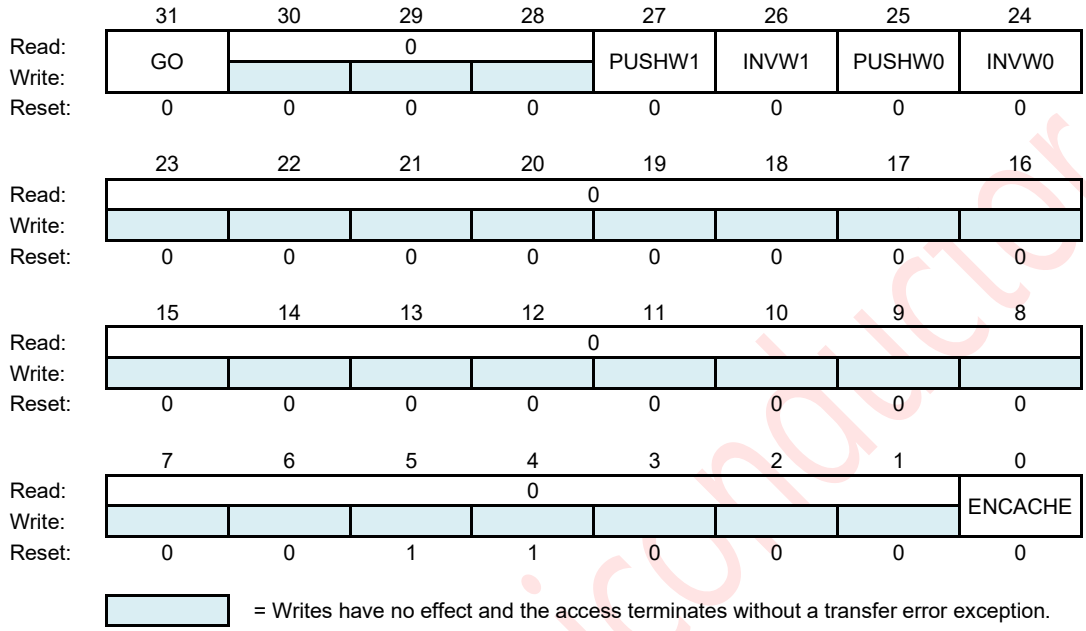


Figure 12-2: Cache Control Register (LMEM_CCR)

GO — Initiate Cache Command
Setting this bit initiates the cache command indicated by bits 27-24. Reading this bit indicates if a command is active. This bit stays set until the command completes. Writing zero has no effect.

1 = Write: initiate command indicated by bits 27-24. Read: cache command active.

0 = Write: no effect. Read: no cache command active.

PUSHW1 — Push way 1

1 = When setting the GO bit, push all modified lines in way 1

0 = no operation

INVW1 — Invalidate way 1.
If the PUSHW0 and INVW0 bits are set, then after setting the GO bit, push all modified lines in way 1 and invalidate all lines in way 1 (clear way 1).

1 = When setting the GO bit, invalidate all lines in way 1.

0 = no operation

PUSHW0 — Push way 0

1 = When setting the GO bit, push all modified lines in way 0

0 = no operation

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INVW0 — Invalidate way 0.
If the PUSHW0 and INVW0 bits are set, then after setting the GO bit, push all modified lines in way 0 and invalidate all lines in way 0 (clear way 0).

1 = When setting the GO bit, invalidate all lines in way 0.

0 = no operation

ENCACHE — Cache enable.

1 = cache is enabled

0 = cache disabled

12.3.2.2. Cache Line Control Register (LMEM_CLCR)

Address: CACHE_BASEADDR+0x0000_0004

	31	30	29	28	27	26	25	24
Read:	0				LACC	LADSEL	LCMD[1:0]	
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0	LCR[2:0]			0			TDSEL
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0	WSEL	CACHE_ADDRESS [13:8]					
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CACHE_ADDRESS [7:2]						0	LGO
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 12-3: Cache Line Control Register (LMEM_CLCR)

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LACC — Line access type.

0 = Read

1 = Write

LADSEL — Line Address Select.

When using the cache address, the way must also be specified in CLCR[WSEL]. When using the physical address, both ways are searched and the command is performed only if a hit.

0 = Cache address

1 = Physical address

LCMD[1:0] — Line command.

00 = Search and read or write.

01 = Invalidate

10 = Push

11 = Clear

LCR[2:0] — Line command current line status.

TDSEL — Tag/Data select. Select tag or data for search and read or write commands.

1 = Tag.

0 = Data.

WSEL — Way select. Select the way of the line commands.

1 = way 1.

0 = way 0.

CACHE_ADDRESS[13:2] — Cache address.

CLCR[13:4] bits are used to access the tag arrays; CLCR[13:2] bits are used to access the data arrays.

LGO — Initiate Cache Line Command.

Setting this bit initiates the cache line command indicated by LMEM_CLCR[27-24]. Reading this bit indicates if a line command is active. This bit stays set until the command completes. Writing zero has no effect. This bit is shared with CSAR[LGO].

1 = Write: initiate line command indicated by bits 27-24. Read: line command active.

0 = Write: no effect. Read: no line command active.

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12.3.2.3. Cache Search Address Register (LMEM_CSAR)

The CSAR register is used to define the explicit cache address or the physical address for line-sized commands specified in the CLCR[LADSEL] bit.

Address: CACHE_BASEADDR+0x0000_0008

	31	30	29	28	27	26	25	24
Read: Write:	Physical_Address[31:24]							
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read: Write:	Physical_Address[23:16]							
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read: Write:	Physical_Address[15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	Physical_Address[7:2]						0	LGO
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 12-4: Cache Search Address Register (LMEM_CSAR)

Physical_Address[31:2] — Physical Address. This represents bits [31:2] of the system address.

Physical_Address[31:14] bits are used for tag compare

Physical_Address[13:4] bits are used to access the tag arrays

Physical_Address[13:2] bits are used to access the data arrays.

LGO — Initiate Cache Line Command.

Setting this bit initiates the cache line command indicated by LMEM_CLCR[27-24]. Reading this bit indicates if a line command is active. This bit stays set until the command completes. Writing zero has no effect.

This bit is shared with CLCR[LGO]

- Write: initiate line command indicated by **LMEM_CLCR[27-24]**. Read: line command active.
- Write: no effect. Read: no line command active.

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12.3.2.4. Cache Read/Write Value Register (LMEM_CCVR)

The CCVR register is used to store the write data or read data for the commands specified in the CLCR register.

Address: CACHE_BASEADDR+0x0000_000C

	31	30	29	28	27	26	25	24
Read: Write:	DATA[31:24]							
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read: Write:	DATA[23:16]							
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read: Write:	DATA[15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	DATA[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 12-5: Cache Read/Write Value Register (LMEM_CCVR)

DATA[31:0] — Cache read/write Data

For tag search, read, or write:

- DATA[31:14] bits are used for tag array R/W value
- DATA[13:4] bits are used for tag set address on reads; unused on writes
- DATA[3:2] bits are reserved

For data search, read. or write:

- DATA[31:0] bits are used for data array R/W value

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12.3.2.5. Cache Access Register (LMEM_ACRG)

The ACRG is used to control the attributes of 10 different memory regions such as write-through, write-back, and non-cacheable.

Address: CACHE_BASEADDR+0x0000_0020

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	R3_CACHEABLE	R3_WT_WB	R2_CACHEABLE	R2_WT_WB	R1_CACHEABLE	R1_WT_WB	R0_CACHEABLE	R0_WT_WB
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 12-6: Cache Access Register (LMEM_ACRG)

Region0: 0x2000_0000 ~ 0x2FFF_FFFF
Region1: 0x6000_0000 ~ 0x6FFF_FFFF
Region2: 0x7000_0000 ~ 0x7FFF_FFFF
Region3: 0x8000_0000 ~ 0x8FFF_FFFF

Rx_CACHEABLE — Region x is cacheable.

1 = cacheable.
0 = non-cacheable

Rx_WT_WB — Region x is write-through if cacheable.

1 = write-back
0 = write-through

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12.3.2.6. Cache Page Invalidation Base Address Register (LMEM_PAGE_INV_BADDR)

Address: CACHE_BASEADDR+0x0000_0180

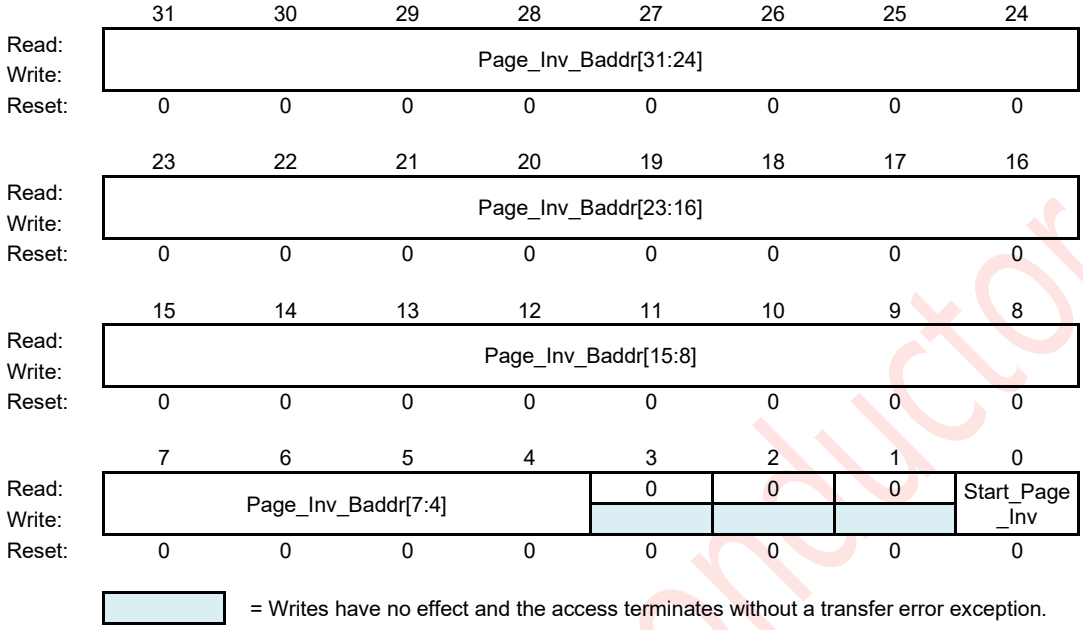


Figure 12-7: Cache Page Invalidate Base Address Register (LMEM_PAGE_INV_BADDR)

Page_Inv_Baddr[31:4] — cache invalidate start address for system memory. Lower 4-bits is ignored because of line alignment.

Start_Page_Inv — start to page invalidate. Cleared if the invalidation is completed.
This bit is shared in bit 0 of LMEM_PAGE_INV_SIZE_REG.

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12.3.2.7. Cache Page Invalidation Base Size Register (LMEM_PAGE_INV_SIZE)

Address: CACHE_BASEADDR+0x0000_0184

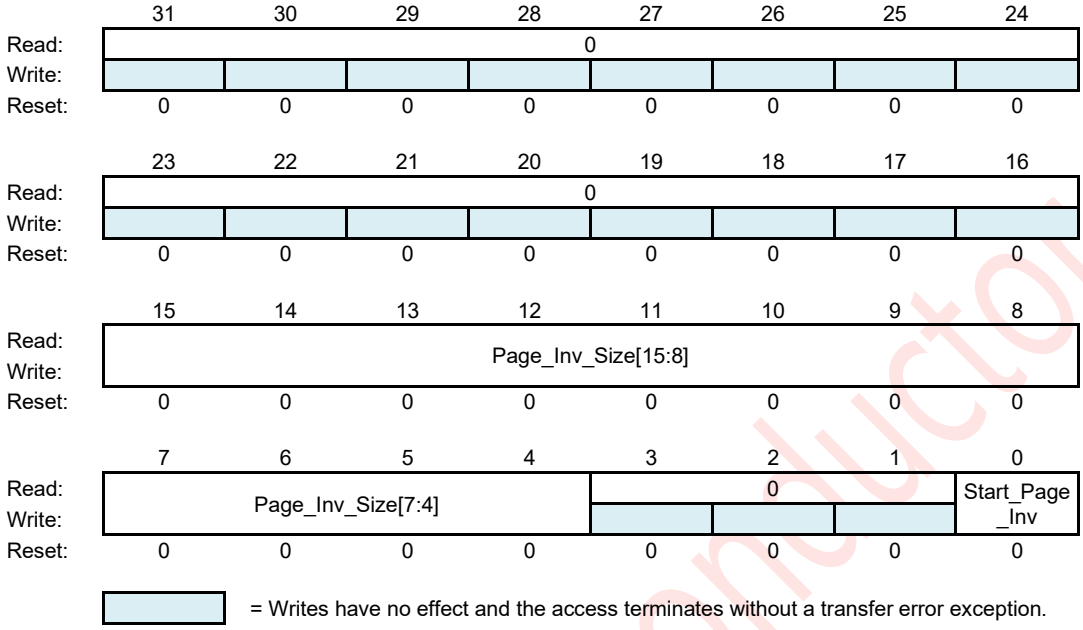


Figure 12-8: Cache Page Invalidate Size Register (LMEM_PAGE_INV_SIZE)

Page_Inv_Size[15:4] — cache invalidate size for system memory. Lower 4-bits is ignored because of line alignment.

Start_Page_Inv — start to page invalidate. Cleared if the invalidation is completed.

This bit is shared in bit 0 of LMEM_PAGE_INV_BADDR_REG.

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12.3.2.8. Cache Clock Enable Register (LMEM_CACHE_CLK_EN)

Address: CACHE_BASEADDR+0x0000_0188

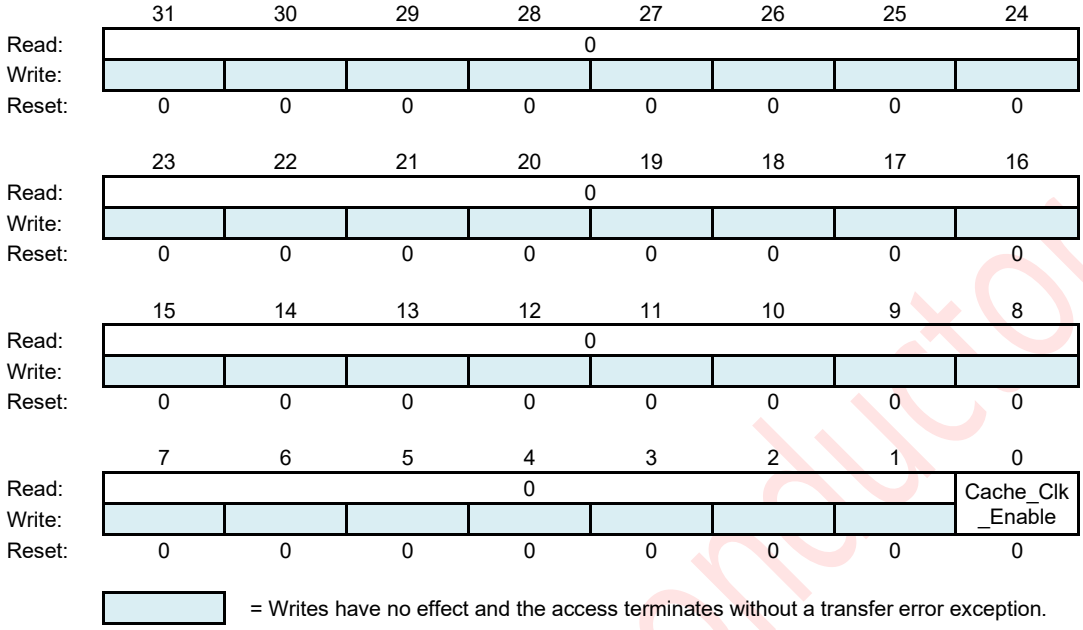


Figure 12-9: Cache Clock Enable Register (LMEM_CACHE_CLK_EN)

Cache_Clk_Enable — cache clock is enabled. Must be '1' if cache is enabled.

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12.4. Cache Function

The caches on this device are structured as follows. Both caches have a 2-way set-associative cache structure with a total size of 32K Bytes. The caches have 32-bits address and data paths, and a 16-byte line size. The cache tags and data storage use external single-port, synchronous RAMs.

For these 32K Bytes caches, each cache TAG function uses two 1024 x 20-bits RAM arrays and the cache DATA function uses two 4096 x 32-bits RAM arrays. The cache TAG entries store 18-bits of upper address as well as a modified and valid bit per cache line. The cache DATA entries store four bytes of code or data.

All normal cache accesses use physical addresses. This leads to the following cache address use:

CACHE - 32K Bytes size = (1024 sets) x (16-byte lines) x (2-way set-associative)

TAG:

- address[31:14] used in tag for compare (hit) logic
- address[13:4] used to select 1 of 1024 sets
- address[3:0] not used

DATA:

- address[31:14] not used
- address[13:4] used to select one of 1024 sets
- address[3:2] used to select one of four 32-bits words within a set
- address[1:0] used to select the byte within the 32-bits word

The caches use a one-cycle parallel TAG and DATA access structure. This structure is aligned in the two stage AHB bus pipeline from the negative edge of the address phase to the negative edge of the data phase:

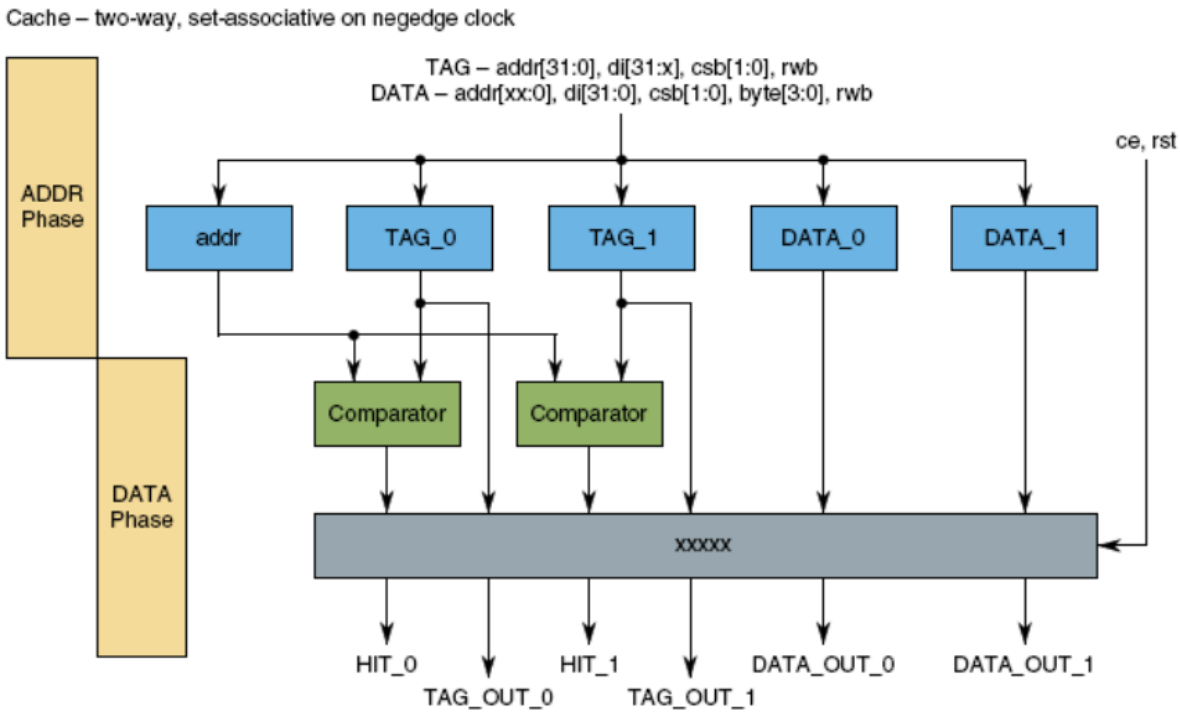


Figure 12-10: Cache Tag and Data Access Structure

On a normal cacheable operation, the full address is registered on the negedge of the address phase in the cache control logic while address bits[12:4] are registered in the TAG arrays, and address bits[12:2] are registered in the DATA arrays. During the full cycle from the negedge of the address phase to the negative edge of the data phase, the TAG and DATA arrays are accessed and cache hit analyzed. For hits, the desired

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read data is returned in the second half of the data phase and writes are done starting on the negedge of the data phase cycle. For misses, the data phase is held as needed while the cache uses its slave bus (CCM, CSM) to access the desired cache line via a line-sized data transfer sent to the crossbar switch.

12.5. Cache Control

The Code and System Caches are disabled at reset. Cache tag and data arrays are not cleared at reset. Therefore, to enable the caches, cache commands must be done to clear and initialize the required tag array bits and to configure and enable the caches.

12.5.1. Cache Set Commands

The cache set commands may operate on:

- All of way 0,
- All of way 1, or
- All of both ways (complete cache).

Cache set commands are initiated using the upper bits in the CCR register. Cache set commands perform their operation on the cache independent of the cache enable bit, CCR[ENCACHE].

A cache set command is initiated by setting the CCR[GO] bit. This bit also acts as a busy bit for set commands. It stays set while the command is active and is cleared by the hardware when the set command completes.

Supported cache set commands are given in **Table 12-2**. Set commands work as follows:

- Invalidate − Unconditionally clear valid and modified bits of a cache entry.
- Push − Push a cache entry if it is valid and modified, then clear the modified bit. If the entry is not valid or not modified, leave it as it is.
- Clear − Push a cache entry if it is valid and modified, then clear the valid and modified bits. If the entry is not valid or not modified, clear the valid bit.

Table 12-2: Cache Set Commands

CCR[27:24]				Command
PUSH W1	INVW1	PUSH W0	INVW0	
0	0	0	0	NOP
0	0	0	1	Invalidate all way 0
0	0	1	0	Push all way 0
0	0	1	1	Clear all way 0
0	1	0	0	Invalidate all way 0
0	1	0	1	Invalidate all way 1; Invalidate all way 0 (invalidate cache)
0	1	1	0	Invalidate all way 1; push all way 0
0	1	1	1	Invalidate all way 1; clear all way 0
1	0	0	0	Push all way 1
1	0	0	1	Push all way 1; Invalidate all way 0
1	0	1	0	Push all way 1; Push all way 0 (push cache)
1	0	1	1	Push all way 1; clear all way 0

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CCR[27:24]				Command
PUSH W1	INVW1	PUSH W0	INVW0	
1	1	0	0	Clear all way 0
1	1	0	1	Clear all way 1; Invalidate all way 0
1	1	1	0	Clear all way 1; push all way 0
1	1	1	1	Clear all way 1; clear all way 0 (clear cache)

After a reset, complete an invalidate cache command before using the cache.

12.5.2. Cache Line Commands

Cache line commands operate on a single line in the cache at a time. Cache line commands can be performed using a physical or cache address.

- A cache address consists of a set address and a way select. The line command acts on the specified cache line.
- Cache line commands with physical addresses first search both ways of the cache set specified by bits [13:4] of the physical address. If they hit, the commands perform their action on the hit way.

Cache line commands are specified using the upper bits in the CLCR register. Cache line commands perform their operation on the cache independent of the cache enable bit (CCR[ENCACHE]). When using a cache address, the command can be completely specified by the CLCR register. When using a physical address, the command must also use the CSAR register to specify the physical address.

A line cache command is initiated by setting the line command go bit (CLCR[LGO] or CSAR[LGO]). This bit also acts as a busy bit for line commands. It stays set while the command is active and is cleared by the hardware when the command completes.

The CLCR[27:24] bits select the line command as follows:

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Table 12-3: **Cache Line Commands**

CLCR[27:24]			Command
LACC	LADSEL	LCMD	
0	0	00	Search by cache address and way
0	0	01	Invalidate by cache address and way
0	0	10	Push by cache address and way
0	0	11	Clear by cache address and way
0	1	00	Search by physical address
0	1	01	Invalidate by physical address
0	1	10	Push by physical address
0	1	11	Clear by physical address
1	0	00	Write by cache address and way
1	0	01	Reserved,NOP
1	0	10	Reserved,NOP
1	0	11	Reserved,NOP
1	1	xx	Reserved,NOP

12.5.2.1. Executing a Series Of Line Commands Using Cache Addresses

A series of line commands with incremental cache addresses can be performed by just writing to the CLCR.

- Place the command in CLCR[27:24],
- Set the way (CLCR[WSEL]) and tag/data (CLCR[TDSEL]) controls as needed,
- Place the cache address in CLCR[CACHEADDR], and
- Set the line command go bit (CLCR[LGO]).

- When one line command completes, initiate the next command by the following steps:
  - Increment the cache address (at bit 2 to step through data or at bit 4 to step through lines), and
  - Set the line command go bit (CLCR[LGO]).

12.5.2.2. Executing a Series of Line Commands Using Physical Addresses

Perform a series of line commands with incremental physical addresses by the following steps:

- Place the command in CLCR[27:24]
- Set the tag/data (CLCR[TDSEL]) control
- Place the physical address in CSAR[PHYADDR] and set the line command go bit(CSAR[LGO]).

When one line command completes, initiate the next command by the following steps:

- Increment the physical address (at bit 2 to step through data or at bit 4 to step through lines), and
- Set the line command go bit (CSAR[LGO]).

The line command go bit is shared between the CLCR and CSAR registers, so that the above steps can be completed in a single write to the CSAR register.

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12.5.2.3. Line Command Results

At completion of a line command, the CLCR register contains information on the initial state of the line targeted by the command. For line commands with cache addresses, this information is read before the line command action is performed from the targeted cache line. For line commands with physical addresses, this information is read on a hit before the line command action is performed from the hit cache line or has initial valid bit cleared if the command misses. In general, if the valid indicator CLCR[LCIVB] is cleared, the targeted line was invalid at the start of the line command and no line operation was performed.

Table 12-4: Line Command Results

CLCR[22:20]			For cache address commands	For physical address commands
LCWY	LCIMB	LCIVB		
0	0	0	Way 0 line Invalid	No hit
0	0	1	Way 0 valid, not modified	Way 0 valid, not modified
0	1	0	Way 0 line was Invalid	No hit
0	1	1	Way 0 valid and modified	Way 0 valid and modified
1	0	0	Way 1 line was Invalid	No hit
1	0	1	Way 1 valid not modified	Way 1 valid not modified
1	1	0	Way 1 line was Invalid	No hit
1	1	1	Way 1 valid and modified	Way 1 valid and modified
4’b1xxx			Bit 23 is available for future use, giving 8 more options if necessary.	

At completion of a line command other than a write, the CCVR (Cache R/W Value Register) contains information on the initial state of the line tag or data targeted by the command. For line commands, CLCR[TDSEL] selects between tag and data. If the line command used a physical address and missed, the data is don't care. For write commands, the CCVR holds the write data.

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13. Direct Memory Access Controller (DMAC)

13.1. Information Specific of DMA Controller

This chapter presents the LT7589's Direct Memory Access Controller.

13.1.1. DMAC Features

- 6 programmable channels to support independent 8, 16, or 32-bits single value or block transfers
- Support of variable sized queues and circular queues
- Source and destination address registers independently configured to post-incrementor remain constant
- Each transfer initiated by peripheral, CPU, periodic timer interrupt or DMA channel request
- Peripheral DMA request sources possible from QSPI, QADC
- Each DMA channel able to optionally send interrupt request to CPU on completion of single value or block transfer
- DMA transfers possible between system memories and all accessible memory mapped locations including peripheral and registers
- DMA supports the following functionality:
  – Scatter Gather
  – Channel Linking
  – Inner Loop Offset
  – Arbitration
    Fixed Group, Fixed Channel
    Round Robin Group, Fixed Channel
    Round Robin Group, Round Robin Channel
    Fixed Group, Round Robin Channel
  – Channel Preemption
  – Cancel Channel Transfer
- Interrupts – The DMA has a single interrupt request for each implemented channel and a combined DMA Error interrupt to flag transfer errors to the system. Each channel DMA interrupt can be enabled or disabled and provides notification of a completed transfer. Refer to the Interrupt Vector in the EIC chapter of the reference manual for the allocation of these interrupts.

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13.1.2. Channel Assignments

The assignments between the DMA requests from the blocks to the channels of the DMA are shown in **Table 13-1.**

Table 13-1: DMA Channel Assignment

DMA Request	Channel	Description
ADC_ISR[EMPTY]	0	qadc_dma_req when the data number in the FIFO is not empty and bit ADC_CFGR1 [DMAEN] is set,
QSPI0 DMA Receive Request	1	QSPI0 dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above DMARDLR[DMARDL] + 1, and DMACR[RDMAE] = 1
QSPI0 DMA Transmit Request	2	QSPI0 dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below DMATDLR[DMATDL], and DMACR[TDMAE] = 1
QSPI1 DMA Receive Request	3	QSPI1 dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above DMARDLR[DMARDL] + 1, and DMACR[RDMAE] = 1
QSPI1 DMA Transmit Request	4	QSPI1 dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below DMATDLR[DMATDL], and DMACR[TDMAE] = 1
QSPI2 DMA Receive Request	5	QSPI2 dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above DMARDLR[DMARDL] + 1, and DMACR[RDMAE] = 1
QSPI2 DMA Transmit Request	6	QSPI2 dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below DMATDLR[DMATDL], and DMACR[TDMAE] = 1
PIT1 DMA Request	7	pit0_dma_req signal is generated when the PIT0 counter reaches 0x0000 and PCSR[PDMAE] = 1
PIT2 DMA Request	8	pit0_dma_req signal is generated when the PIT0 counter reaches 0x0000 and PCSR[PDMAE] = 1
PIT3 DMA Request	9	pit0_dma_req signal is generated when the PIT0 counter reaches 0x0000 and PCSR[PDMAE] = 1
SCI0 TX DMA Request	10	sci0_tx_req signal is generated when the number of datawords in the transmit FIFOis equal to or less than the number indicated by SCI_WATER[TXWATER])
SCI0 RX DMA Request	11	sci0_rx_req signal is generated when the number of datawords in the receive buffer is greater than the number indicated by SCI_WATER[RXWATER]
SCI1 TX DMA Request	12	sci1_tx_req signal is generated when the number of datawords in the transmit FIFOis equal to or less than the number indicated by SCI_WATER[TXWATER])
SCI1 RX DMA Request	13	sci1_rx_req signal is generated when the number of datawords in the receive buffer is greater than the number indicated by SCI_WATER[RXWATER]
SCI2 TX DMA Request	14	sci2_tx_req signal is generated when the number of datawords in the transmit FIFOis equal to or less than the number indicated by SCI_WATER[TXWATER])
SCI2 RX DMA Request	15	sci2_rx_req signal is generated when the number of datawords in the receive buffer is greater than the number indicated by SCI_WATER[RXWATER]

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13.2. Introduction

The direct memory access controller (DMA) is capable of performing complex data movements through 16 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes a DMA engine that performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation minimizes the overall block size.

Figure 13-1 is a block diagram of the DMA module.

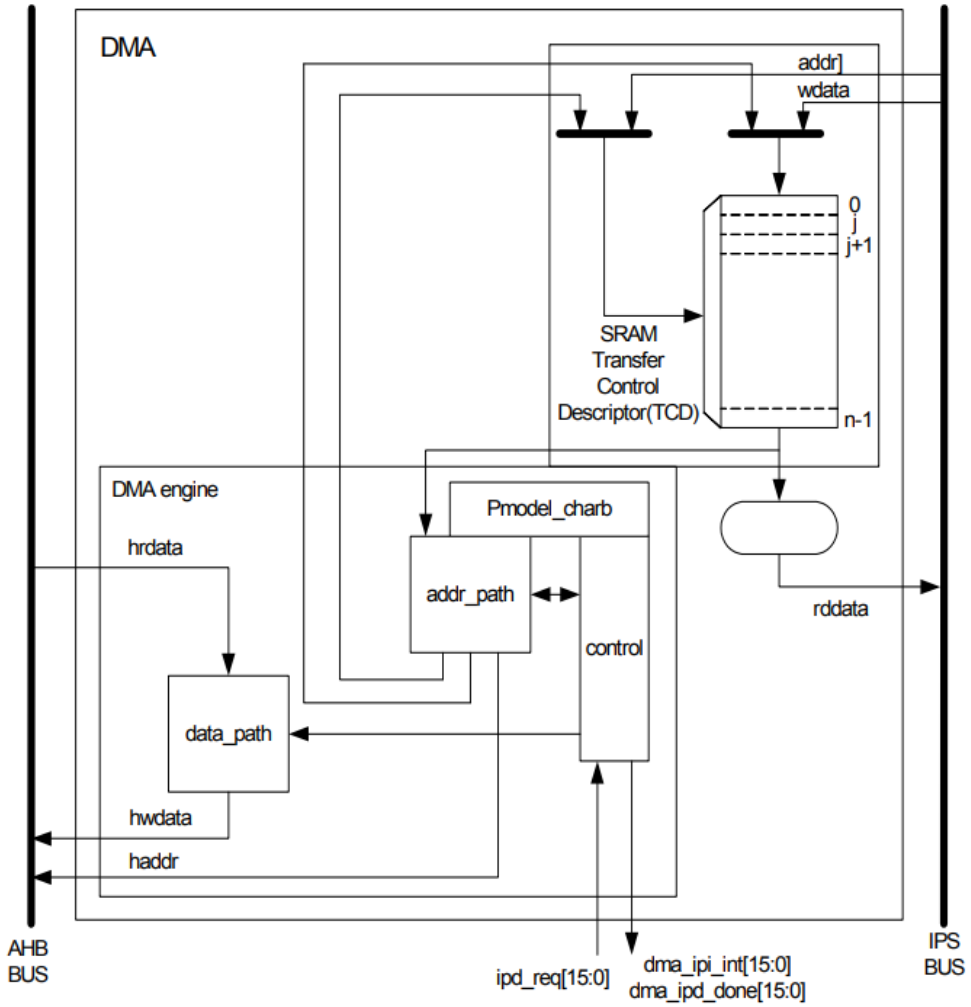


Figure 13-1: DMA Block Diagram

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13.2.1. Features

The DMA module supports the following features:

- All data movement via dual-address transfers: read from source, write to destination
  – Programmable source, destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
  – An inner data transfer loop is defined by a “minor” byte transfer count
  – An outer data transfer loop is defined by a “major” iteration count
- Channel service request via one of three methods:
  – Explicit software initiation
  – Initiation via a channel-to-channel linking mechanism for continuous transfers. Independent channel linking at end of minor loop and/or major loop
  – Peripheral-paced hardware requests (one per channel)
  – For all three methods, one service request per execution of the minor loop is required
- Support for fixed-priority and round-robin channel arbitration
- Channel completion is reported via optional interrupt requests
  – One interrupt per channel, optionally asserted at completion of major iteration count
  – Error terminations are optionally enabled per channel, and logically summed together to form a small number of error interrupt outputs
- Support scatter/gather DMA processing
- Support complex data structures
- Support cancelling transfers via software or hardware

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14. Option Byte (OPB)

14.1. Memory Map and Registers

14.1.1. Memory Map

The Option Byte memory map is shown in **Table 14-1**, and its base address is 0x4012_0000 which is the same as the Efuse Module.

Table 14-1: Register Memory Map

Address Offset	Bits[31:24]	Bits[23:16]	Bits[15:8]	Bits[7:0]	Access[1,2]
0x001C	CCR		PVDC		S
0x0020	PLLOCKCR		EOSCST		S
0x0024	PVDFEVR		RFEVR		S
0x002C	FCR		Reserved3		S
0x0030	Reserved				S
0x0034	LDOTCR	VREFTCR	ADCCDISR		S
0x0038	RTCTCR		Reserved		S

Notes:

1. S = CPU supervisor mode access only.
2. Accessing to supervisor-only address locations in user mode has no effect and result in a cycle termination transfer error.
3. Writes to reserved address locations have no effect and reads return 0s.

14.1.2. Register Descriptions

14.1.2.1. Programmable Voltage Detector Configuration Register (PVDC)

Address: EFM_BASEADDR+0x0000_001C

	15	14	13	12	11	10	9	8
Read:	PVDF	PVDPORRE	PVDTEST[1:0]		PVDOE	PVDRE	PVDIE	PVDE
Write:								
Reset:	0	Note1	0	0	1	Note1	0	1

	7	6	5	4	3	2	1	0
Read:	0						PVDC[1:0]	
Write:								
Reset:	0	0	0	0	0	0	Note1	Note1

= Writes have no effect and the access terminates without a transfer error exception.

Note1: Determined by the value of FUSE Area

Figure 14-1: Programmable Voltage Detector Configuration Register (PVDC)

PVDF — Programmable Voltage Detector Flag

The PVDF indicates if VDD is lower than PVD threshold. POR can clear it.

1 = VDD33 is lower than PVD threshold

0 = VDD33 is not lower than PVD threshold

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PVDPORRE — Program Voltage Detector (PVD) Power-On Reset Enable

The PVDPORRE shows whether Program Voltage Detector Power-On reset is enable or not. When enabled, RSR[POR] flag will be set after PVD reset. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is loaded from the corresponding bit of FUSE area after power-on. This bit can be set by software after power on reset.

1 = PVD will generate Power-On reset when VDD33 is lower than PVD threshold

0 = PVD will NOT generate Power-On reset when VDD33 is lower than PVD threshold

PVDTEST[1:0] — Write Access Enable Sequence Input

The PVDC register can not be changed, unless the correct sequence is written. The right sequence is: 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the PVDC register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

PVDOE — Programmable Voltage Detector Output Enable

1 = PVD Output Enable

0 = PVD Output Disable

PVDRE — Program Voltage Detector (PVD) Reset Enable

The PVDRE shows whether Program Voltage Detector reset is enable. The default value is loaded from the FUSE area. When enabled and PVDPORRE is disabled, RSR[PVDF] flag will be set after PVD reset. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is loaded from the corresponding bit of FUSE area after power-on. This bit can be changed by software after power on reset.

1 = PVD reset is enabled

0 = PVD reset is disabled

PVDIE — Programmable Voltage Detector Interrupt Enable

The PVDIE is used to check if VCC is lower than PVD threshold

1 = If VCC is lower than PVD threshold, an interrupt will be generated

0 = If VCC is not lower than PVD threshold, no interrupt will be generated.

PVDE — Programmable Voltage Detector Enable

The PVDE determines whether PVD is enabled or not. POR can clear it.

1 = Enable PVD

0 = Disable PVD

PVDC[1:0] — Programmable Voltage Detector Configuration Value.

Table 14-2: Programmable Voltage Detector

PVDC	Detect Voltage
2'b00	2.16V
2'b01	2.32V
2'b10	2.48V
2'b11	2.64V

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The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, PVDC[1:0] will be cleared after power on reset, otherwise if the content in corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. These bits can be changed by software after power on reset.

14.1.2.2. Customer Configuration Register (CCR)

Address: EFM_BASEADDR+0x0000_001E

	15	14	13	12	11	10	9	8
Read:	RGBEN	0	RTC_INTERFACE_EN	PGMDIS	RSTOUTDIS	CLKOUTDIS	RTC_INTERFACE_LVD_ISOEN	QSPI2EN
Write:								
Reset:	0	0	0	Note1	Note1	Note1	0	0

	7	6	5	4	3	2	1	0
Read:	0	0	ADCCSPOR	PVDCE	0	EOSCSTE	CCRTEST[1:0]	
Write:								
Reset:	0	0	Note1	Note1	0	Note1	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Note1: Determined by the value of FUSE Areas

Figure 14-2: Customer Configuration Register (CCR)

RGBEN — RGB Interface Enable Control Bit

The RGBEN determines whether the RGB Interface is enabled or not.

1 = RGB Interface is enabled

0 = RGB Interface is disabled

Table 14-3: RGB Interface Enable Control

RGB Disabled	RGB Enabled
EBI_D[15:0]	TFT_RGB[15:0]
EBI_WR#	TFT_VS
EBI_RD#	TFT_HS
EBI_RS	TFT_DE
EBI_CS#	TFT_PCLK

RTC_INTERFACE_EN — This bit determines whether the RTC analog module can be reconfigured or not when PRCSR[Dir] or PRENR[RTC_EN_Dir] is set.

1 = RTC analog module can be reconfigured.

0 = RTC analog module can not be reconfigured.

PGMDIS — Programming Debug Interface Disable Bit

The PGMDIS shows whether the Programming Debug Interface is disabled or not. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit will be set after power-on.

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This bit can be changed by software after power on reset.

1 = Programming debug function is disabled

0 = Programming debug function is enabled

Table 14-4: Programming Debug Interface Control

Programming Enabled	Programming Disabled
PGMCK	RXD2
PGMIO	TXD2

RSTOUTDIS — RSTOUT Disable Bit

The RSTOUTDIS shows whether the RSTOUT pin function is disabled and INT1[6] is enabled. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit will be set after power-on. This bit can be changed by software after power on reset.

1 = RSTOUT Pin function is disabled

0 = RSTOUT Pin function is enabled

Table 14-5: RSTOUT Disable Control

RSTOUT Enabled	RSTOUT Disabled
RSTOUT	INT1[6]

CLKOUTDIS — CLKOUT Disable Bit

The CLKOUTDIS shows whether the CLKOUT pin function is disabled and INT1[0] is enabled. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit will be set after power-on. This bit can be changed by software after power on reset.

1 = CLKOUT Pin function is disabled

0 = CLKOUT Pin function is enabled

Table 14-6: CLKOUT Disable Control

CLKOUT Enabled	CLKOUT Disabled
CLKOUT	INT1[0]

RTC_INTERFACE_LVD_ISOEN — This bit determines whether the RTC analog interface will be isolated or not when Program Voltage Detector event happens.

1 = RTC analog interface will not be isolated when Low voltage happens.

0 = RTC analog interface will be isolated when Low voltage happens.

QSPI2EN — QSPI2 Interface Enable Control Bit

The QSPI2EN determines whether the QSPI2 Interface is enabled or not.

1 = QSPI2 Interface is enabled

0 = QSPI2 Interface is disabled

Table 14-7: QSPI2 Interface Enable Control

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QSPI2 Disabled	QSPI2 Enabled
PWM0[0]	QSCS2#
PWM0[1]	QSCK2
PWM0[2]	QSIO2[0]
PWM0[3]	QSIO2[1]
PWM1[0]	QSIO2[2]
PWM1[1]	QSIO2[3]

ADCCSPOR — ADC Channel Setting Bit after power-on

The ADCSPOR shows whether ADCCDISR[ADCCDIS] is loaded from FUSE area or not after power on. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = ADCCDISR[ADCCDIS] is loaded from FUSE area after Power on

0 = ADCCDISR[ADCCDIS] is not loaded from FUSE area after Power on

PVDCE — Program Voltage Detector (PVD) Configuration Enable

The PVDCE shows whether Program Voltage Detector configuration is loaded from FUSE area or not after power on. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = PVD configuration is loaded from FUSE Area after Power on

0 = PVD configuration is not loaded from FUSE Area after Power on

EOSCSTE — External High Speed Oscillator Stable Time Configuration Enable

The EOSCSTE shows whether External High Speed Oscillator Stable Time configuration is loaded from FUSE Area after power on. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = External High Speed Oscillator(FXOSC) Stable Time configuration is loaded from FUSE Area after Power on

0 = External High Speed Oscillator(FXOSC) Stable Time configuration is not loaded from FUSE Area after Power on

CCRTEST[1:0] — Write Access Enable Sequence Input

The writable bit of CCR register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of CCR register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

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14.1.2.3. External High Speed Oscillator Stable Time Configuration Register (EOSCST)

Address: EFM_BASEADDR+0x0000_0020

	15	14	13	12	11	10	9	8
Read:	EOSCTEST[1:0]		0	0	EOSCST[11:8]			
Write:								
Reset:	0	0	0	0	Note1	Note1	Note1	Note1

	7	6	5	4	3	2	1	0
Read:	EOSCST[7:0]							
Write:								
Reset:	Note1	Note1	Note1	Note1	Note1	Note1	Note1	Note1

= Writes have no effect and the access terminates without a transfer error exception.

Note1: Determined by the value of FUSE Area

Figure 14-3: External High Speed Oscillator Stable Time Configuration Register (EOSCST)

EOSCTEST[1:0] — Write Access Enable Sequence Input

The writable bit of EOSCST register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11.After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of EOSCST register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

EOSCST[11:0] — External High Speed Oscillator Stable Time Value.

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the value of EOSCST[11:0] is 12'h3ff after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. Software can change it after power on reset. After External Oscillator is enabled, it will wait EOSCST[11:0] cycles of 128KHz oscillator and then the gate of the clock will be turn-on.

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14.1.2.4. PLL Lock Time Configuration Register (PLLOCKCR)

Address: EFM_BASEADDR+0x0000_0022

	15	14	13	12	11	10	9	8
Read:	PLLST[15:14]		PLLST[13:8]					
Write:	PLLTEST[1:0] / PLLST[15:14]							
Reset:	0	0	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
Read: Write:	PLLST[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 14-4: PLL Lock Time Configuration Register (PLLOCKCR)

PLLST[15:0] — PLL Lock Time Value.

After enabled, the PLL will wait PLLST[15:0] cycles of External High speed oscillator (FXOSC) and then the gate of the clock will be turn-on.

PLLTEST[1:0] — Write Access Enable Sequence Input

The PLLST register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the PLLST register can be changed at will. Any writes can clear these two bits when the value equals to 2'b11.

Note: PLLST[15:14] is writable only when the value of PLLTEST[1:0] equals to 2'b11.

14.1.2.5. RESET Pin Filter Enable and Value Register (RFEVR)

Address: EFM_BASEADDR+0x0000_0024

	15	14	13	12	11	10	9	8
Read:	0	0	RFEVRTEST[1:0]		0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	RFV[7:0]							
Reset:	Note1	Note1	Note1	Note1	Note1	Note1	Note1	Note1

= Writes have no effect and the access terminates without a transfer error exception.

Note1: Determined by the value of FUSE Area

Figure 14-5: RESET Pin Filter Enable and Value Register (RFEVR)

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RFEVRTEST [1:0] — Write Access Enable Sequence Input

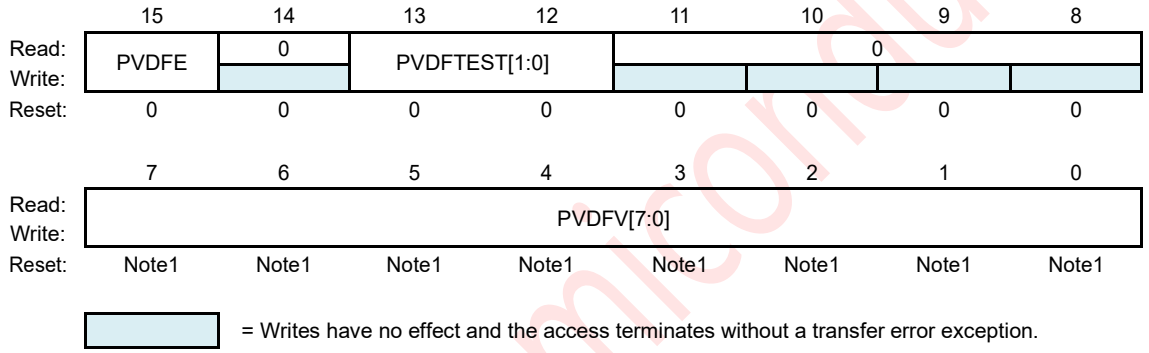
The writable bit of RFEVR register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of RFEVR register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

RFV[7:0] — RESET Pin Filter Value

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the value of RFV[7:0] is 8'h0d after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. These bits can be changed by software after power on reset.

14.1.2.6. Programmable Voltage Detector Filter Enable and Value Register (PVDFEVR)

Address: EFM_BASEADDR+0x0000_0026



Note1: Determined by the value of FUSE Area

Figure 14-6: Programmable Voltage Detector Filter Enable and Value Register (PVDFEVR)

PVDFE — Programmable Voltage Detector Filter Enable.

The PVDFE shows whether Program Voltage Detector Filter is enabled. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the PVDFE is cleared after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. This bit can be changed by software after power on reset.

1 = PVD filter is enabled

0 = PVD filter is disabled

PVDFTEST[1:0] — Write Access Enable Sequence Input

The writable bit of PVDFEVR register can not be changed, unless the correct sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of PVDFEVR register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

PVDFV[7:0] — Programmable Voltage Detector Filter Value

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the value of PVDFV[7:0] is 8'h0 after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. These bits can be changed after power on reset.

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14.1.2.7. Factory Configuration Register (FCR)

Address: EFM_BASEADDR+0x0000_002E

	15	14	13	12	11	10	9	8
Read:	0	0	RTCTE	TMDIS	RESETFTE	LDO1P2TE	VREF1P2TE	PVDFTE
Write:								
Reset:	0	0	Note1	Note1	Note1	Note1	Note1	Note1

	7	6	5	4	3	2	1	0
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Note1: Determined by the value of FUSE Area

Figure 14-7: Factory Configuration Register (FCR)

RTCTE — RTC Bias/Cap rimming Enable

The RTCTE shows whether RTC Bias or Capacitance is trimmed or not. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = RTC Bias or Capacitance is trimmed

0 = RTC Bias or Capacitance is not trimmed

TMDIS — Test Mode Disable Bit

The TMDIS shows whether test mode (except STB) is disabled or not. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = Test mode is disabled

0 = Test mode is enabled

RESETFTE — Reset Pin Filter Trimming Enable

The RESETFTE shows whether Reset Pin Filter is trimmed or not. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = Reset Pin Filter is trimmed

0 = Reset Pin Filter is not trimmed

LDO1P2TE — LDO1P2 Trimming Enable

The LDO1P2TE shows whether LDO1P2 is trimmed or not. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = LDO1P2 is trimmed

0 = LDO1P2 is not trimmed

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VREF1P2TE — VREF1P2 Module Trimming Configuration Register

The VREF1P2TE shows whether VREF1P2 Module is trimmed or not. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = Internal VREF1P2 Module is trimmed

0 = Internal VREF1P2 Module is not trimmed

PVDFTE — PVD Filter Trimming Enable

The PVDFTE shows whether PVD Filter is trimmed or not. The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, this bit is cleared, otherwise if the content in the corresponding FUSE area is matched, this bit is set after power-on.

1 = PVD Filter is trimmed

0 = PVD Filter is not trimmed

14.1.2.8. Channel Disable Configuration Register (ADCCDISR)

Address: EFM_BASEADDR+0x0000_0034

	15	14	13	12	11	10	9	8
Read:	ADCCDISTEST[1:0]		0					
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	ADCCDIS[7:0]							
Write:								
Reset:	Note1	Note1	Note1	Note1	Note1	Note1	Note1	Note1

= Writes have no effect and the access terminates without a transfer error exception.

Note1: Determined by the value of FUSE Area

Figure 14-8: ADC Channel Disable Configuration Register (ADCCDISR)

ADCCDISTEST[1:0] — Write Access Enable Sequence Input

The writable bits ADDCDIS[7:0] can not be changed until the correct seguences are written into ADCCDISTEST. The right sequence are : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of ADCCDISTEST register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

ADCCDIS[7:0] — ADC Channel Disable Configuration

ADCCDIS[7:0] determine whether AIN[7:0] are used as ADC channel or GPIO. If the corresponding FUSE area is in an erased status, these bits are cleared and ADC channel function is valid, otherwise if the content in the corresponding FUSE area is matched, ADCCDIS[7:0] are loaded from the FUSE area. These bits can be changed after power on reset.

Table 14-8: ADC Channel Disable Control

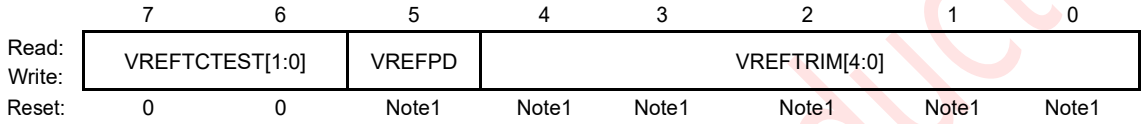
ADC Channel Disabled	ADC Channel Enabled
INT0[0]	AIN[0]
INT0[1]	AIN[1]
INT0[2]	AIN[2]

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ADC Channel Disabled	ADC Channel Enabled
INT0[3]	AIN[3]
INT0[4]	AIN[4]
INT0[5]	AIN[5]
INT0[6]	AIN[6]
INT0[7]	AIN[7]

14.1.2.9. VREF1P2 Trimming Configuration Register (VREFTCR)

Address: EFM_BASEADDR+0x0000_0036



Note1: Determined by the value of FUSE Area

Figure 14-9: VREF Trimming Configuration Register (VREFTCR)

VREFTCTEST[1:0] — WSFTCR Write Access Sequence In

The writable bit of VREFTCTEST register can not be changed, unless the correct data sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of VREFTCTEST register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

VREFPD — Internal VREF1P2 Module Power Down. The setup time is 10us after Internal VREF1P2 Module is turn on.

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the VREFPD is set after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. This bit can be changed by software after power on reset.

1 = Internal VREF1P2 Module Power Down

0 = Internal VREF1P2 Module Power On

VREFTRIM[4:0] — VREF1P2 Module Trimming Value

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the VREFTRIM[4:0] is 5'h18 after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. These bits can be changed by software after power on reset.

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14.1.2.10. LDO1P2 Trimming Configuration Register (LDOTCR)

Address: EFM_BASEADDR+0x0000_0037

	7	6	5	4	3	2	1	0
Read:	LDO1P2TC[7:6]		LDO1P2TC[5:0]					
Write:	LDO1P2TEST[1:0] / LDO1P2TC[7:6]							
Reset:	Note1	Note1	Note1	Note1	Note1	Note1	Note1	Note1

Note1: Determined by the value of FUSE Area

Figure 14-10: LDO1P2 Trimming Configuration Register (LDOTCR)

LDO1P2TC[7] — LDO over-current limit function control bit

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the LDO1P2TC[7] is 1'b0 after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. This bit can be changed after power on reset.

1 = LDO over-current limit function will be turned off.

0 = LDO over-current limit function will be turned on.

LDO1P2TC[6] — LDO1P2 power down control bit

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the LDO1P2TC[6] is 1'b0 after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. This bit can be changed after power on reset.

1 = LDO1P2 will be power down.

0 = LDO1P2 will be power on.

LDO1P2TC[5:0] — LDO1P2 Trimming Value

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the LDO1P2TC[5:0] is 6'h00 after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. These bits can be changed by software after power on reset.

LDO1P2TEST[1:0] — LDO1P2TC Write Access Sequence In

The writable bit of LDO1P2TC register can not be changed, unless the correct data sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of LDO1P2TC register can be changed at will. Any writes can clear these two bits when the value equals to 2'b11.

Note: LDO1P2TC[7:6] is writable only when the value of LDO1P2TEST[1:0] equals to 2'b11.

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14.1.2.11. RTC Trimming Configuration Register (RTCTCR)

Address: EFM_BASEADDR+0x0000_003A

	15	14	13	12	11	10	9	8
Read:	RTCTCTEST[1:0]		0				RTC_TEST_MODE	Trim_Load
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	RTC_BIAS_TRIM[3:0]				RTC_CAP_TRIM[3:0]			
Write:								
Reset:	Note1	Note1	Note1	Note1	Note1	Note1	Note1	Note1

= Writes have no effect and the access terminates without a transfer error exception.

Note1: Determined by the value of FUSE Area

Figure 14-11: RTC Trimming Configuration Register (RTCTCR)

RTCTCTEST[1:0] — RTCTC Write Access Sequence In

The writable bit of RTCTC register can not be changed, unless the correct data sequence is written. The right sequence is : 2'b01 → 2'b10 → 2'b11. After writing these two bits by this sequence, these two bits' value == 2'b11, then the writable bit of RTCTC register can be changed at will. Writing 2'b00 can clear these two bits when the value equals to 2'b11. Writing other values has no effect and returns 2'b11.

RTC_TEST_MODE — RTC Test Mode enable.

1 = RTC Test Mode is enabled.

0 = RTC Test Mode is disabled.

Trim_Load — Low to high edge will latch RTC_BIAS_TRIM and RTC_CAP_TRIM value into RTC analog module.

RTC_BIAS_TRIM[3:0] — RTC Oscillator Bias Trimming configuration bits.

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the RTC_BIAS_TRIM[3:0] is 4'b0111 after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. These bits can be changed by software after power on reset.

RTC_CAP_TRIM[3:0] — RTC Oscillator Load Capacitance C1 and C2 Trimming configuration bits.

The default value is loaded from the FUSE area. If the corresponding FUSE area is in an erased status, the RTC_BIAS_TRIM[3:0] is 4'b1100 after power on reset, otherwise if the content in the corresponding FUSE area is matched, these bits are loaded from the FUSE area after power-on. These bits can be changed by software after power on reset.

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15. Programmable Interrupt Timer (PIT)

15.1. Introduction

LT7589's Programmable Interrupt Timer (PIT) is a 16-bits timer that provides precise interrupts at regular intervals with minimal processor intervention. The timer can either count down from the value written in the modulus latch, or it can be a free-running down-counter.

15.2. Block Diagram

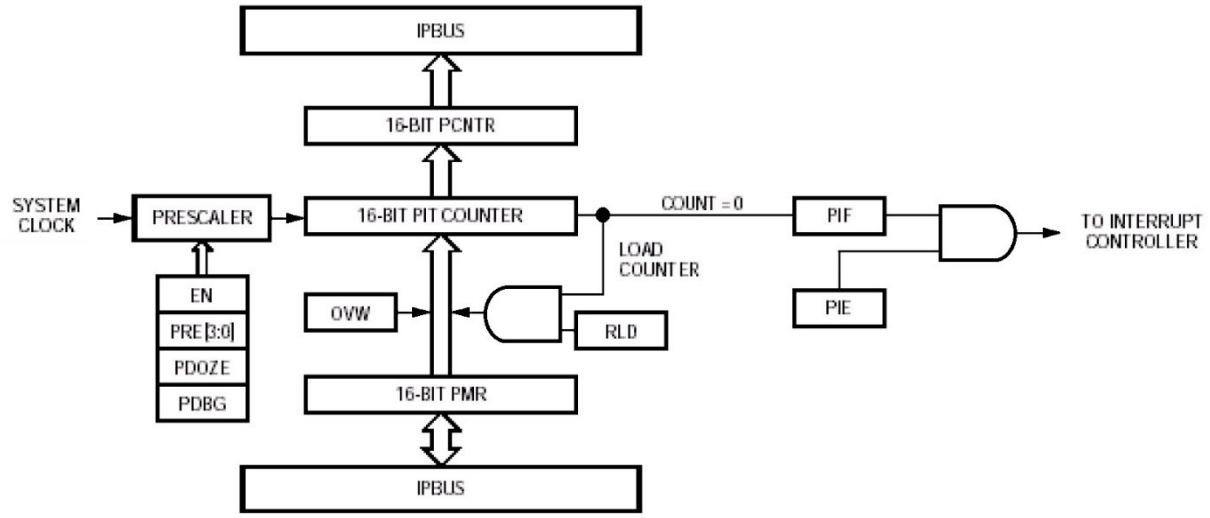


Figure 15-1: PIT Block Diagram

15.3. Modes of Operation

This subsection describes the three low-power modes and the debug mode.

15.3.1. Wait Mode

In wait mode, the PIT module continues to operate normally and can be configured to exit the low-power mode by generating an interrupt request.

15.3.2. Doze Mode

In doze mode with the PDOZE bit set in the PIT Control and Status Register (PCSR), PIT module operation stops. In doze mode with the PDOZE bit clear, doze mode does not affect PIT operation. When doze mode is exited, PIT operation continues from the state it was in before entering doze mode.

15.3.3. Stop Mode

In stop mode, the system clock is absent, and PIT module operation stops.

15.3.4. Debug Mode

In debug mode with the PDBG bit set in PCSR, PIT module operation stops. In debug mode with the PDBG bit cleared, debug mode does not affect PIT operation. When debug mode is exited, PIT operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain.

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15.4. Signals

The PIT module has no off-chip signals.

15.5. Memory Map and Registers

This subsection describes the memory map and register structure for PIT. The PIT Module memory map is shown in **Table 15-1**. The PIT0 base address is 0x4004_0000, PIT1 is 0x4005_0000, PIT2 is 0x4006_0000, and PIT3 is 0x4007_0000.

15.5.1. Memory Map

Refer to **Table 15-1** for a description of the memory map.

This device has four programmable interrupt timers.

Table 15-1: **Programmable Interrupt Timer Module Memory Map**

PITn Address	Bits[15:0]	Access(1)
0x0	PIT Modulus Register (PMR)	S
0x2	PIT Control and Status Register (PCSR)	S
0x4	Unimplemented(2)	—
0x6	PIT Count Register (PCNTR)	S/U

Notes:

(1) S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. Accessing to supervisor only addresses in user mode has no effect and result in a cycle termination transfer error.

(2) Accesses to unimplemented address locations have no effect and result in a cycle termination transfer error.

15.5.2. Register Descriptions

The PIT programming model consists of below registers:

- The PIT Control and Status Register (PCSR) configures the timer's operation. See **Section 15.5.2.2**.
- The PIT Modulus Register (PMR) determines the timer modulus reload value. See **Section 15.5.2.1**.
- The PIT Count Register (PCNTR) provides visibility to the counter value. See **Section 0.**

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15.5.2.1. PIT Modulus Register (PMR)

The 16-bits read/write PIT Modulus Register (PMR) contains the timer modulus value for loading into the PIT counter when the count reaches 0x0000 and the RLD bit is set.

When the OVW bit is set, PMR is transparent, and the value written to PMR is immediately loaded into the PIT counter. The prescaler counter is reset anytime a new value is loaded into the PIT counter and also during reset. Reading the PMR returns the value written in the modulus latch. Reset initializes PMR to 0xFFFF.

Address: PITn_BASEADDR+0x0000_0000

	15	14	13	12	11	10	9	8
Read: Write:	PM[15:8]							
Reset:	1	1	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
Read: Write:	PM[7:0]							
Reset:	1	1	1	1	1	1	1	1

Figure 15-2: PIT Modulus Register (PMR)

15.5.2.2. PIT Control and Status Register (PCSR)

Address: PITn_BASEADDR+0x0000_0002

	15	14	13	12	11	10	9	8
Read:	0				PRE[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	PDMAE	PDOZE	PDBG	OVW	PIE	PIF	RLD	EN
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 15-3: PIT Control and Status Register (PCSR)

PRE[3:0] — Prescaler Bits

The read/write PRE[3:0] bits select the system clock divisor to generate the PIT clock as **Table 15-2** shows.

To accurately predict the timing of the next count, change the PRE[3:0] bits only when the enable bit (EN) is cleared. Changing the PRE[3:0] resets the prescaler counter. System reset and the loading of a new value into the counter also reset the prescaler counter. Setting the EN bit and writing to PRE[3:0] can be done in this same write cycle. Clearing the EN bit stops the prescaler counter.

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Table 15-2: Prescaler Select Encoding

PRE[3:0]	IPS Clock Divisor
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1,024
1011	2,048
1100	4,096
1101	8,192
1110	16,384
1111	32,768

PDMAE — DMA Enable Control Bit

The read/write PDMAE bit controls whether a dma request will be generated or not when the PIT counter reaches 0x0000.

1 = Dma request will be generated when the PIT counter reaches 0x0000.

0 = Dma request will not be generated when the PIT counter reaches 0x0000.

PDOZE — Doze Mode Bit

The read/write PDOZE bit controls the function of the PIT in doze mode. Reset clears PDOZE.

1 = PIT function is stopped in doze mode

0 = PIT function is not affected in doze mode

When doze mode is exited, timer operation continues from the state it was in before entering doze mode.

PDBG — Debug Mode Bit

The read/write PDBG bit controls the function of the PIT in debug mode. Reset clears PDBG.

1 = PIT function is stopped in debug mode

0 = PIT function is not affected in debug mode

During debug mode, register read and write accesses function normally. When debug mode is exited, timer operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain.

Note: Changing the PDBG bit from 1 to 0 during debug mode starts the PIT timer. Likewise, changing the PDBG bit from 0 to 1 during debug mode stops the PIT timer.

OVW — Overwrite Bit

The read/write OVW bit enables writing to PMR to immediately overwrite the value in the PIT counter.

1 = Writing PMR immediately replaces value in PIT counter.

0 = Value in PMR replaces value in PIT counter when the count reaches 0x0000.

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PIE — PIT Interrupt Enable Bit

The read/write PIE bit enables the PIF flag to generate interrupt requests.

1 = PIF interrupt requests is enabled

0 = PIF interrupt requests is disabled

PIF — PIT Interrupt Flag

The read/write PIF flag is set when the PIT counter reaches 0x0000. Clear PIF by writing a 1 to it or by writing to PMR or acknowledged by DMA request. Writing 0 has no effect. Reset clears PIF.

1 = PIT count has reached 0x0000.

0 = PIT count has not reached 0x0000.

RLD — Reload Bit

The read/write RLD bit enables loading the value of PMR into the PIT counter when the count reaches 0x0000.

1 = Counter is reloaded from PMR on count of 0x0000

0 = Counter rolls over to 0xFFFF on count of 0x0000

EN — PIT Enable Bit

The read/write EN bit enables PIT operation. When the PIT is disabled, the counter and prescaler are held in a stopped state.

1 = PIT is enabled

0 = PIT is disabled

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15.5.2.3. PIT Count Register (PCNTR)

The 16-bits, read-only PIT Control Register (PCNTR) contains the counter value.

Reading the 16-bits counter with two 8-bits reads is not guaranteed to be coherent.

Writing to PCNTR has no effect, and write cycles are terminated normally.

Address: PITn_BASEADDR+0x0000_0006

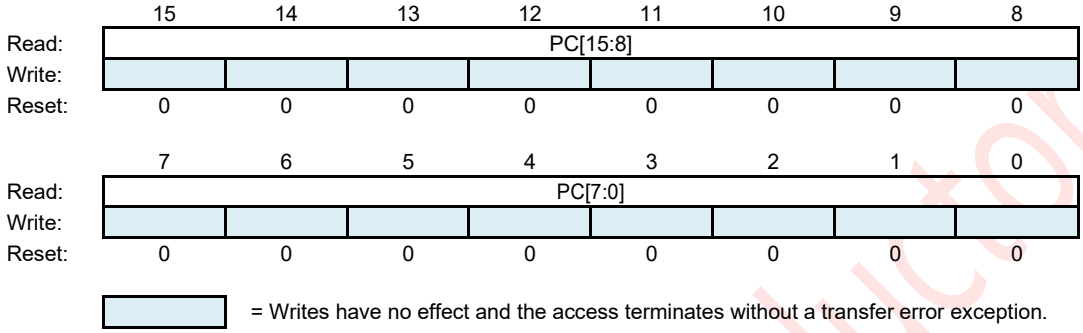


Figure 15-4: PIT Count Register (PCNTR)

15.6. Functional Descripiton

This subsection describes the PIT functional operation.

15.6.1. Set-and-Forget Timer Operation

This mode of operation is selected when the RLD bit in the PCSR register is set.

When the PIT counter reaches a count of 0x0000, the PIF flag is set in PCSR. The value in the modulus latch is loaded into the counter, and the counter begins decrementing toward 0x0000. If the PIE bit is set in PCSR, the PIF flag issues an interrupt request to the CPU.

When the OVW bit is set in PCSR, the counter can be directly initialized by writing to PMR without having to wait for the count to reach 0x0000.

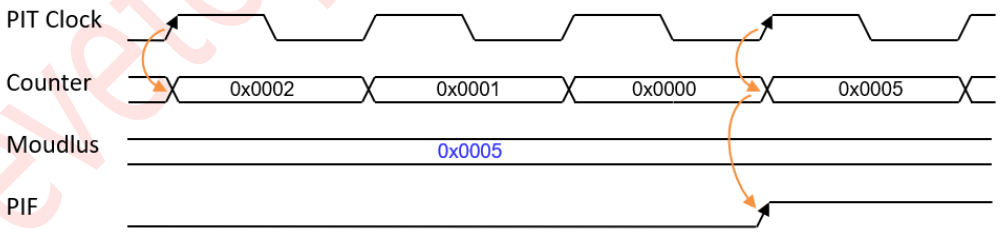


Figure 15-5: Counter Reloading from the Modulus Latch

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15.6.2. Free-Running Timer Operation

This mode of operation is selected when the RLD bit in PCSR is cleared. In this mode, the counter rolls over from 0x0000 to 0xFFFF without reloading from the modulus latch and continues to decrement.

When the counter reaches a count of 0x0000, the PIF flag is set in PCSR. If the PIE bit is set in PCSR, the PIF flag issues an interrupt request to the CPU.

When the OVW bit is set in PCSR, the counter can be directly initialized by writing to PMR without having to wait for the count to reach 0x0000.

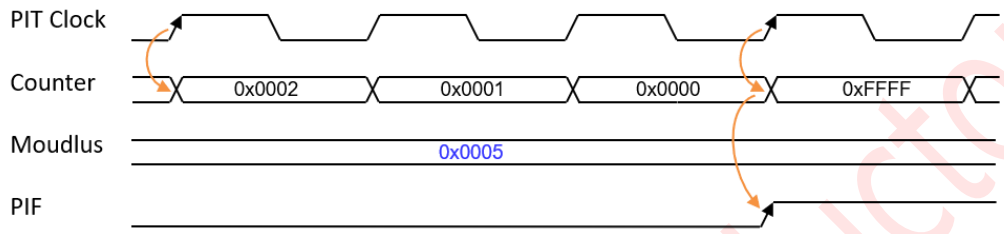


Figure 15-6: Counter in Free-Running Mode

15.6.3. Timeout Specifications

The 16-bits PIT counter and prescaler supports different timeout periods. The prescaler divides the system clock as selected by the PRE[3:0] bits in PCSR. The PM[15:0] bits in PMR select the timeout period.

timeout period = PRE[3:0] x (PM[15:0] + 1) clocks

15.7. Interrupt Operation

Table 15-3 lists the interrupt requests generated by the PIT.

Table 15-3: PIT Interrupt Requests

Interrupt Request	Flag	Enable Bit
Timeout	PIF	PIE

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16. Watchdog Timer (WDT)

16.1. Introduction

LT7589's Watchdog Timer is a 16-bits timer used to help software recover from runaway code or give an interrupt when the operation has run longer than expected. The watchdog timer has a free-running down-counter (watchdog counter) that generates a reset or interrupt on underflow. To prevent a reset, software must periodically restart the countdown by servicing the watchdog.

16.2. Modes of Operation

This subsection describes the operation of the watchdog timer in low-power modes and debug mode of operation.

16.2.1. Wait Mode

In wait mode with the WAIT bit set in the Watchdog Control Register (WCR), watchdog timer operation stops. In wait mode with the WAIT bit cleared, the watchdog timer continues to operate normally.

16.2.2. Doze Mode

In doze mode with the DOZE bit set in WCR, watchdog timer module operation stops. In doze mode with the DOZE bit cleared, the watchdog timer continues to operate normally.

16.2.3. Stop Mode

In stop mode with the STOP bit set in WCR, watchdog operation stops in stop mode. When stop mode is exited, the watchdog operation continues operation from the state it was in prior to entering stop mode. In stop mode with the STOP bit cleared, the watchdog timer continues to operate normally.

16.2.4. Debug Mode

In debug mode with the DBG bit set in WCR, watchdog timer module operation stops. In debug mode with the DBG bit cleared, the watchdog timer continues to operate normally. When debug mode is exited, watchdog timer operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain.

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16.3. Block Diagram

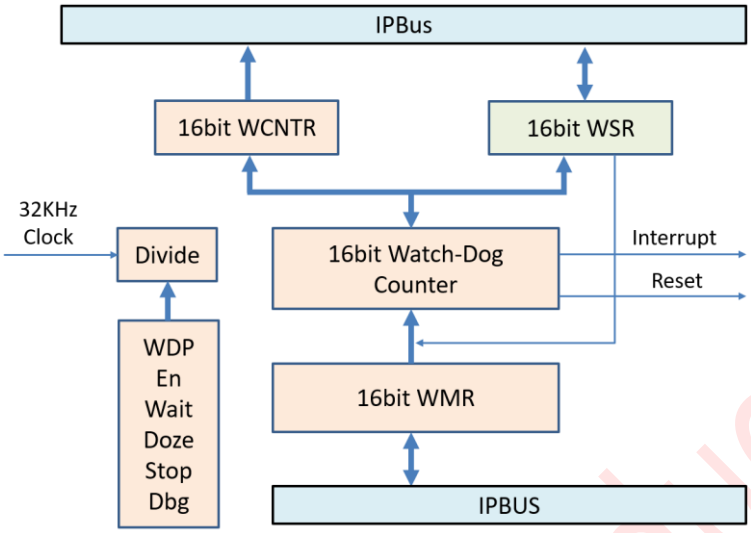


Figure 16-1: Watchdog Timer Block Diagram

16.4. Signals

The watchdog timer module has no off-chip signals.

16.5. Memory Map and Registers

This subsection describes the memory map and registers for the Watchdog Timer. The WDT Module base address is 0x4013_0000.

16.5.1. Memory Map

Refer to **Table 16-1** for an overview of the watchdog memory map.

Table 16-1: Watchdog Timer Module Memory Map

Offset Address	Bits[15:0]	Access(1)
0x0000	Watchdog Modulus Register (WMR)	S
0x0002	Watchdog Control Register (WCR)	S
0x0004	Watchdog Service Register (WSR)	S/U
0x0006	Watchdog Count Register (WCNTR)	S/U

Note (1) : S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. Accessing to supervisor only addresses in user mode has no effect and result in a cycle termination transfer error.

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16.5.2. Register Description

The watchdog timer programming model consists of these registers:

- The Watchdog Control Register (WCR) configures watchdog timer operation. See **Section 16.5.2.2**.
- The Watchdog Modulus Register (WMR) determines the timer modulus reload value. See **Section 16.5.2.1.**
- The Watchdog Count Register (WCNTR) provides visibility to the watchdog counter value. See **Section 16.5.2.4.**
- The Watchdog Service Register (WSR) requires a service sequence to prevent reset. The read-only WC[15:0] field reflects the current value in the watchdog counter. Reading the 16-bits WCNTR with two 8-bits reads is not guaranteed to return a coherent value. Writing to WCNTR has no effect, and write cycles are terminated normally. This register is for watchdog work domain, so the read value may not be stable, please read it time after time continuously..

16.5.2.1. Watchdog Modules Register (WMR)

Address: WDT_BASEADDR+0x0000_0000

	15	14	13	12	11	10	9	8
Read: Write:	WM[15:8]							
Reset:	1	1	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
Read: Write:	WM[7:0]							
Reset:	1	1	1	1	1	1	1	1

Figure 16-2: Watchdog Modulus Register (WMR)

WM[15:0] — Watchdog Modulus Field

WM[15:0] field contains the modulus that is reloaded into the watchdog counter by a service sequence. Writing to WMR immediately loads the new modulus value into the watchdog counter. The new value is also used at the next and all subsequent reloads.

Reading WMR returns the value in the modulus register. Reset initializes the WM[15:0] field to 0xFFFF.

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16.5.2.2. Watchdog Control Register (WCR)

The 16-bits read/write Watchdog Control Register (WCR) configures watchdog timer operation.

Address: WDT_BASEADDR+0x0000_0002

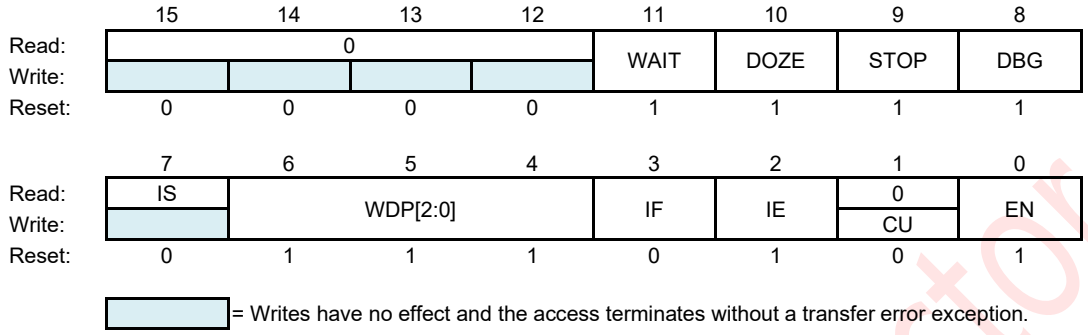


Figure 16-3: Watchdog Control Register (WCR)

WAIT — Wait Mode Bit

WAIT bit controls the function of the watchdog timer in wait mode. Reset sets WAIT.

1 = Watchdog timer is stopped in wait mode

0 = Watchdog timer is not affected in wait mode

DOZE — Doze Mode Bit

DOZE bit controls the function of the watchdog timer in doze mode. Reset sets DOZE.

1 = Watchdog timer is stopped in doze mode

0 = Watchdog timer is not affected in doze mode

STOP — STOP Mode Bit

STOP bit controls the function of the watchdog timer in stop mode. Reset sets STOP.

1 = Watchdog timer is stopped in stop mode

0 = Watchdog timer is not affected in stop mode

DBG — Debug Mode Bit

DBG bit controls the function of the watchdog timer in debug mode. During debug mode, watchdog timer registers can be written and read normally. When debug mode is exited, timer operation continues from the state it was in before entering debug mode, but any updates made in debug mode remain.

1 = Watchdog timer is stopped in debug mode

0 = Watchdog timer is not affected in debug mode

Note:

Changing the DBG bit from 1 to 0 during debug mode starts the watchdog timer.
Changing the DBG bit from 0 to 1 during debug mode stops the watchdog timer.

IS — Watchdog Clock Domain Interrupt Status Bit

This bit is read-only, if this bit is 1’b1, the status of watchdog clock domain is not cleared, so if CPU wants to sleep or stop, it will be wakeup again. Therefore, before CPU wants to sleep or stop, check this bit first.

WDP[2:0] — Watchdog Timer Prescaler

The WDP[2:0] bits determine the watchdog timer prescaling when the watchdog timer is running. The different prescaling values and their corresponding time-out periods are shown in **Table 16-2** Watchdog Timer Prescaler.

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Table 16-2: Watchdog Timer Prescaler

WDP[2:0]	Prescaler
000	128KHz / 2048
001	128KHz / 1024
010	128KHz / 512
011	128KHz / 256
100	128KHz / 128
101	128KHz / 64
110	128KHz / 32
111	128KHz / 16

IF — Watchdog Interrupt Flag Bit

Write One to this bit will clear the flag.

IE — Watchdog Interrupt Enable Bit

IE bit enables the watchdog timer interrupt mode. Once interrupt is generated and the EN bit is 1, this bit will be auto cleared.

1 = Watchdog timer interrupt mode is enabled

0 = Watchdog timer interrupt mode is disabled

CU — Watchdog Change Update Bit

Writing One to CU bit will update the WDP[2:0] and WMR to the work latch.

EN — Watchdog Enable Bit

EN bit enables the watchdog timer.

1 = Watchdog timer is enabled

0 = Watchdog timer is disabled

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16.5.2.3. Watchdog Service Register (WSR)

When the watchdog timer is enabled, writing 0x5555 and then 0xAAAA to the Watchdog Service Register (WSR) before the watchdog counter times out prevents a reset. If WSR is not serviced before the timeout, the watchdog timer sends a signal to the reset controller or interrupt controller module and asserts a system reset or interrupt.

Both writes must occur in the order listed before the timeout, but any number of instructions can be executed between the two writes. However, writing any value other than 0x5555 or 0xAAAA to WSR resets the servicing sequence, both values are required to be written to prevent the watchdog timer from causing a reset.

Address: WDT_BASEADDR+0x0000_0004

	15	14	13	12	11	10	9	8
Read: Write:	WS[15:8]							
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	WS[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 16-4: Watchdog Service Register (WSR)

16.5.2.4. Watchdog Count Register (WCNTR)

Address: WDT_BASEADDR+0x0000_0006

	15	14	13	12	11	10	9	8
Read:	WC[15:8]							
Write:								
Reset:	1	1	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
Read:	WC[7:0]							
Write:								
Reset:	1	1	1	1	1	1	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 16-5: Watchdog Count Register (WCNTR)

WC[15:0] — Watchdog Count Field

The read-only WC[15:0] field reflects the current value in the watchdog counter. Reading the 16-bits WCNTR with two 8-bits reads is not guaranteed to return a coherent value. Writing to WCNTR has no effect, and write cycles are terminated normally. This register is for watchdog work domain, so the read value may not be stable, please read it time after time continuously.

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17. Real Time Controller (RTC)

17.1. Introduction

LT7589's Real Time Controller controls a comprehensive PMU with RTC function. It can reconfigure RTC counter, set alarms, and generate time/alarm interrupts.

17.2. Features

The main features of the module:

– Reconfigure RTC counter and read from seconds, minutes, hours and days counters

– Support alarm settings

– Interrupt Sources: second, minute, hour, day interrupts, programmable alarm interrupts, 1KHz/32KHz periodic interrupts .

17.3. Test Mode

In test mode, RTC can be configured by CPU or by chip pins, and RTC status and clock signals can be checked by chip pins.

17.4. Block Diagram

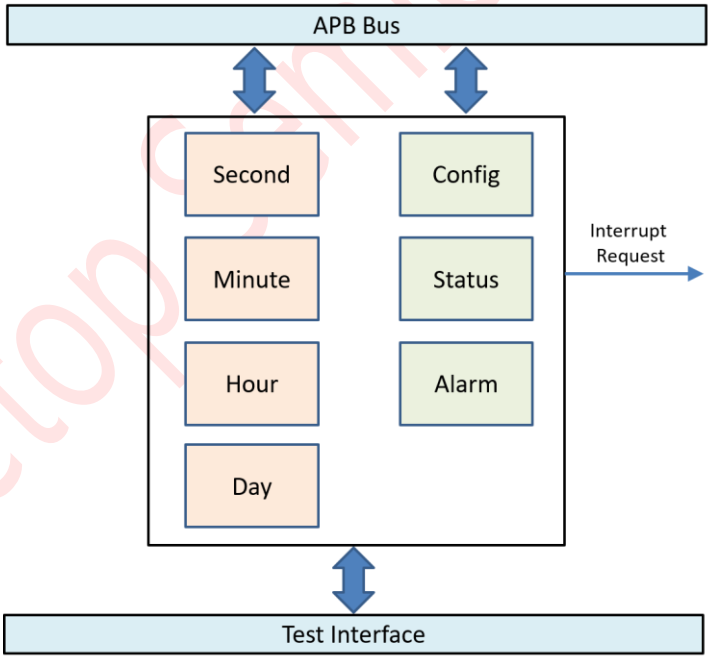


Figure 17-1: RTC Block Diagram

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17.5. Application Circuit

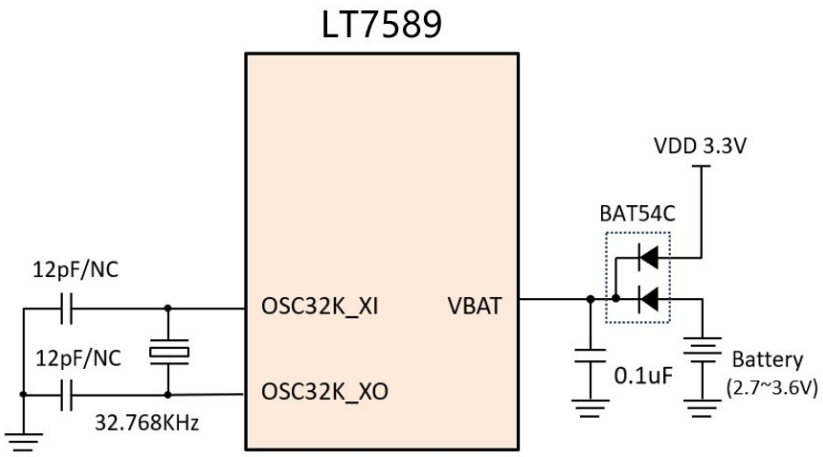


Figure 17-2: RTC Application Circuit

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18. Edge Port Module (EPORT)

18.1. Introduction

LT7589 has three Edge Port Modules (EPORT). And each EPORT has eight corresponding external interrupt pins. Each pin can be configured individually as a low level-sensitive interrupt pin, an edge-detecting interrupt pin (rising edge, falling edge, or both), or a general-purpose input/output/ (I/O) pin. See **Figure 18-1**.

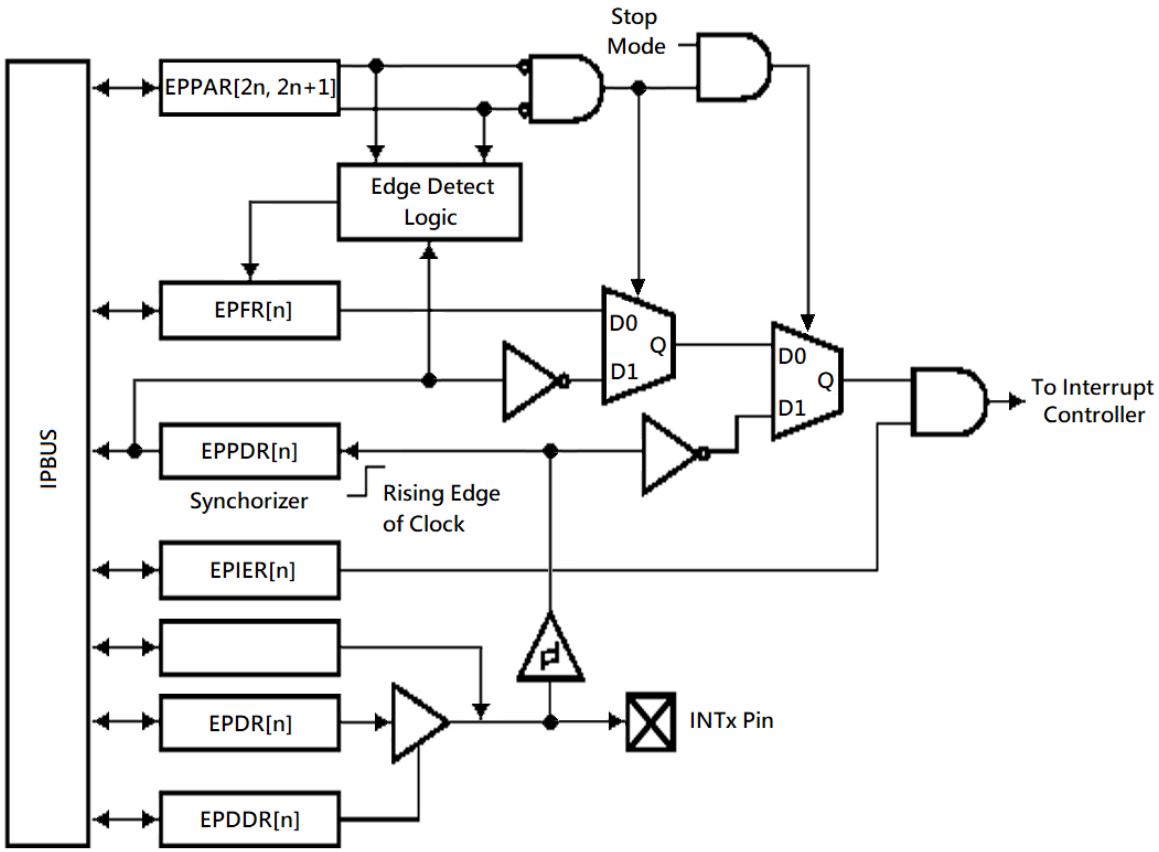


Figure 18-1: EPORT Block Diagram

18.2. Low-Power Mode Operation

This subsection describes the operation of the EPORT module in low-power modes.

18.2.1. Wait and Doze Modes

In wait and doze modes, the EPORT module continues to operate normally and may be configured to exit the low-power modes by generating an interrupt request on either a selected edge or a low level on an external pin.

18.2.2. Stop Mode

In stop mode, there is no clocks available to perform the edge-detect function. Only the level-detect logic is active (if configured) to allow any low level on the external interrupt pin to generate an interrupt (if enabled) to exit stop mode.

Note: The input pin synchronizer is bypassed for the level-detect logic since no clocks is available.

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18.3. Interrupt/General-Purpose I/O Pin Descriptions

All pins default to general-purpose input pins at reset. The pin value is synchronized to the rising edge of CLKOUT when reading from the EPORT Pin Data Register (EPPDR). The values used in the edge/level detect logic are also synchronized to the rising edge of CLKOUT. These pins use Schmitt triggered input buffers which have built in hysteresis designed to decrease the probability of generating false edge-triggered interrupts for slow rising and falling input signals.

18.4. Memory Map And Registers

The EPORT Module memory map is shown in **Table 18-1**. The EPORT0 base address is 0x400F_0000, EPORT1 is 0x4010_0000, and EPORT2 is 0x401D_0000. This subsection describes the memory map and register structure.

18.4.1. Memory Map

Refer to **Table 18-1** for a description of the EPORT memory map.

Table 18-1: Module Memory Map

Address Offset	Bits[15:8]	Bits[7:0]	Access(1)
0x0000	EPORT Data Direction Register (EPDDR)	EPORT Interrupt Enable Register (EPIER)	S
0x0002	EPORT Pin Assignment Register (EPPAR)		S
0x0004	EPORT Flag Register (EPFR)	EPORT Pin Pull-up enable Register (EPPUE)	S/U
0x0006	EPORT Data Register (EPDR)	EPORT Pin Data Register (EPPDR)	S/U
0x0008	EPORT Digital Filter Control Register (EPFC)	EPORT Bit Set Register (EPBSR)	S
0x000A	EPORT Level Polarity Register (EPLPR)	EPORT Open Drain Register (EPODE)	S
0x000C	Reserved		S
0x000E	EPORT Bit Clear Register (EPBCR)	Reserved	S

Note (1) : S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. Accessing to supervisor only addresses in user mode has no effect and result in a cycle termination transfer error.

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18.4.2. Register Description

The EPORT programming model consists of below registers:

- The EPORT Pin Assignment Register (EPPAR) controls the function of each pin individually.
- The EPORT Data Direction Register (EPDDR) controls the direction of each one of the pins individually.
- The EPORT Interrupt Enable Register (EPIER) enables interrupt requests for each pin individually.
- The EPORT Data Register (EPDR) holds the data to be driven to the pins.
- The EPORT Pin Data Register (EPPDR) reflects the current state of the pins.
- The EPORT Flag Register (EPFR) individually latches EPORT edge events.
- The EPORT Pin Pull-up Enable Register (EPPUE) controls the pull-up of each one of the pins individually.
- The EPORT Level Polarity Register (EPLPR) controls the level polarity of each one of the pins for level-sensitive.
- The EPORT Open Drain Enable Register (EPODE) controls the Open Drain of each one of the pins for output individually.
- The EPORT Digital Filter Control Register(EPFC) enables the filter and controls the width of input pulse that will be filtered.

18.4.2.1. Edge Port Interrupt Enable Register (EPIER)

Address: EPORTn_BASEADDR+0x0000_0000

	7	6	5	4	3	2	1	0
Read: Write:	EPIE[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 18-2: EPORT Port Interrupt Enable Register (EPIER)

EPIE[7:0] — Edge Port Interrupt Enable Bits

The read/write EPIE[7:0] bits enable EPORT interrupt requests. If a bit in EPIER is set, EPORT generates an interrupt request when:

- The corresponding bit in the EPORT Flag Register (EPFR) is set or later becomes set, or
- The corresponding pin level is low and the pin is configured for level-sensitive operation

Clearing a bit in EPIER negates any interrupt request from the corresponding EPORT pin. Reset clears EPIE[7:0].

1 = Interrupt requests from corresponding EPORT pin is enabled

0 = Interrupt requests from corresponding EPORT pin is disabled

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18.4.2.2. Eport Data Direction Register (EPDDR)

Address: EPORTn_BASEADDR+0x0000_0001

	7	6	5	4	3	2	1	0
Read: Write:	EPDD[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 18-3: EPORT Data Direction Register (EPDDR)

EPDD[7:0] — Edge Port Data Direction Bits

Setting any bit in the EPDDR configures the corresponding pin as an output. Clearing any bit in EPDDR configures the corresponding pin as an input. Pin direction is independent of the level/edge detection configuration. Reset clears EPDD[7:0].

To use an EPORT pin as an external interrupt request source, its corresponding bit in EPDDR must be clear. Software can generate interrupt requests by programming the EPORT Data Register when the EPDDR selects output.

1 = Corresponding EPORT pin is configured as output

0 = Corresponding EPORT pin is configured as input

18.4.2.3. Eport Pin Assignment Register (EPPAR)

Address: EPORTn_BASEADDR+0x0000_0002

	15	14	13	12	11	10	9	8
Read: Write:	EPPA7[1:0]		EPPA6[1:0]		EPPA5[1:0]		EPPA4[1:0]	
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	EPPA3[1:0]		EPPA2[1:0]		EPPA1[1:0]		EPPA0[1:0]	
Reset:	0	0	0	0	0	0	0	0

Figure 18-4: EPORT Pin Assignment Register (EPPAR)

EPPAx[1:0] — EPORT Pin Assignment Select Fields

The read/write EPPAx fields configure EPORT pins for level detection and rising and/or falling edge detection as shown in Table 18-2.

Pins configured as level-sensitive are inverted so that a logic 0 or logic 1 on the external pin represents a valid interrupt request. Level-sensitive interrupt inputs are not latched. To guarantee that a level-sensitive interrupt request is acknowledged, the interrupt source must keep the signal asserted until acknowledged by software. Level sensitivity must be selected to bring the device out of stop mode with an INTx interrupt.

Pins configured as edge-triggered are latched and need not remain asserted for interrupt generation. A pin configured for edge detection is monitored no matter it is configured as input or output.

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Table 18-2: EPPAx Field Settings

EPPAx	Pin Configuration
00	Pin INTx level-sensitive
01	Pin INTx rising edge triggered
10	Pin INTx falling edge triggered
11	Pin INTx both falling edge and rising edge triggered

Interrupt requests generated in the EPORT module can be masked by the interrupt controller module. EPPAR functionality is independent of the selected pin direction.

Reset clears the EPPAx fields.

18.4.2.4. Eport Pin Pull-up Enable Register (EPPUE)

Address: EPORTn_BASEADDR+0x0000_0004

	7	6	5	4	3	2	1	0
Read: Write:	EPPUE[7:0]							
Reset:	1	1	1	1	1	1	1	1

Figure 18-5: EPORT Pin Pull-up enable Register (EPPUE)

EPPUE[7:0] — Edge Port Pin Pull-up enable Bits

Setting any bit in the EPPUE configures the corresponding pin to enable pull-up. The setting is available only when EPORT are in input mode. Clearing any bit in EPPUE configures the corresponding pin to disable pull-up.

Reset sets EPPUE[7:0].

1 = Corresponding EPORT pin configured to enable pull-up

0 = Corresponding EPORT pin configured to disable pull-up

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18.4.2.5. Edge Port Flag Register (EPFR)

Address: EPORTn_BASEADDR+0x0000_0005

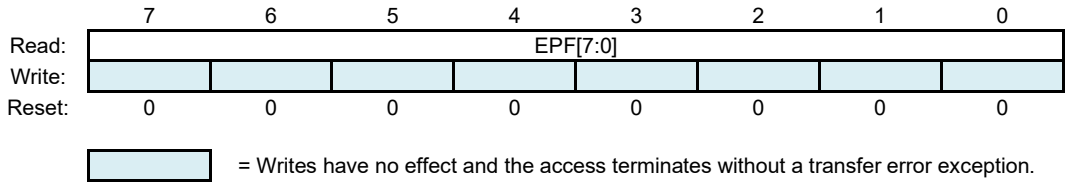


Figure 18-6: EPORT Port Flag Register (EPFR)

EPF[7:0] — Edge Port Flag Bits

When an EPORT pin is configured for edge triggering, its corresponding read/write bit in EPFR indicates that the selected edge has been detected. Reset clears EPF[7:0].

1 = Selected edge for INTx pin has been detected.

0 = Selected edge for INTx pin has not been detected.

Bits in this register are set when the selected edge is detected on the corresponding pin. A bit remains set until cleared by writing a 1 to it. Writing 0 has no effect. If a pin is configured as level-sensitive (EPPARx = 00), pin transitions do not affect this register.

18.4.2.6. Edge Port Pin Data Register (EPPDR)

Address: EPORTn_BASEADDR+0x0000_0006

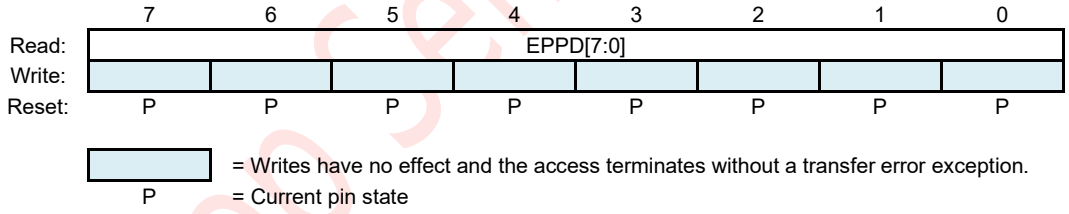


Figure 18-7: EPORT Port Pin Data Register (EPPDR)

EPPD[7:0] — Edge Port Pin Data Bits

The read-only EPPDR reflects the current state of the EPORT pins. Writing to EPPDR has no effect, and the write cycle terminates normally. Reset does not affect EPPDR.

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18.4.2.7. Edge Port Data Register (EPDR)

Address: EPORTn_BASEADDR+0x0000_0007

	7	6	5	4	3	2	1	0
Read: / Write:	EPD[7:0]							
Reset:	1	1	1	1	1	1	1	1

Figure 18-8: EPORT Port Data Register (EPDR)

EPD[7:0] — Edge Port Data Bits

Data written to EPDR is stored in an internal register; if any pin of the port is configured as an output, the bit stored for that pin is driven onto the pin. Reading EDPR returns the data stored in the register. Reset sets EPD[7:0].

18.4.2.8. Eport Port Bit Set Register (EPBSR)

Address: EPORTn_BASEADDR+0x0000_0008

	7	6	5	4	3	2	1	0
Read:	0							
Write:	EPBSR[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 18-9: EPORT Port Bit Set Register (EPBSR)

EPBSR[7:0] — EPORT Port Bit Set Register

1 = The corresponding bit of EPDR will be set;

0 = The corresponding bit of EPDR will not be effected;

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18.4.2.9. Eport Digital Filter Control Register (EPFC)

Address: EPORTn_BASEADDR+0x0000_0009

	7	6	5	4	3	2	1	0
Read: Write:	Filter_Width[6:0]							Filter_En
Reset:	0	0	0	0	0	0	0	0

Figure 18-10: EPORT Digital Filter Control Register (EPFC)

Filter_Width[6:0] — EPORT Digital Filter Pulse Width Select Bit

Filter_Width[6:0] determine the width of the input pulse to be filtered. If the input pulse width is less than (Filter_Width[6:0]+2), the pulse will be filtered.

Filter_En — EPORT Digital Filter Enable Bit

1 = EPORT digital filter is enabled;

0 = EPORT digital filter is disabled;

18.4.2.10. Eport Open Drain Enable Register (EPODE)

Address: EPORTn_BASEADDR+0x0000_000A

	7	6	5	4	3	2	1	0
Read: Write:	EPODE[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 18-11: EPORT Open Drain Enable Register (EPODE)

EPODE[7:0] — Edge Port Open Drain enable Bits

If EPORT are configured to output, setting any bit in the EPODE configures the corresponding pin to Open Drain output. Clearing any bit in EPODE configures the corresponding pin to CMOS output. Reset clears EPODE[7:0].

1 = Corresponding EPORT pin is configured to Open Drain output

0 = Corresponding EPORT pin is configured to CMOS output

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18.4.2.11. Eport Level Polarity Register (EPLPR)

Address: EPORTn_BASEADDR+0x0000_0000B

	7	6	5	4	3	2	1	0
Read: Write:	EPLPR[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 18-12: EPORT Level Polarity Register (EPLPR)

EPLPR[7:0] — Edge Port Level Polarity Bits

If EPORT are configured to level-sensitive, setting any bit in the EPLPR configures the corresponding pin high level-sensitive. Clearing any bit in EPLPR configures the corresponding pin low level-sensitive. Reset clears EPLPR[7:0].

1 = Corresponding EPORT pin is configured to high level-sensitive

0 = Corresponding EPORT pin is configured to low level-sensitive

18.4.2.12. Eport Port Bit Clear Register (EPBCR)

Address: EPORTn_BASEADDR+0x0000_000F

	7	6	5	4	3	2	1	0
R	0							
W	EPBCR[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 18-13: EPORT Port Bit Clear Register (EPBCR)

EPBCR[7:0] — EPORT Port Bit Clear Register

1 = The corresponding bit of EPDR will be cleared;

0 = The corresponding bit of EPDR will not be effected;

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19. CANBus Controller(CANBC)

19.1. Introduction

LT7589's CANBus module is a communication controller implementing the CAN protocol based on the CAN 2.0B protocol specification. A general block diagram is shown in **Figure 19-1**, which describes the main sub-blocks implemented in the CANBus module, including two embedded memories, one for storing Message Buffers (MB) and another one for storing Rx Individual Mask Registers. The functions of the submodules are described in subsequent sections.

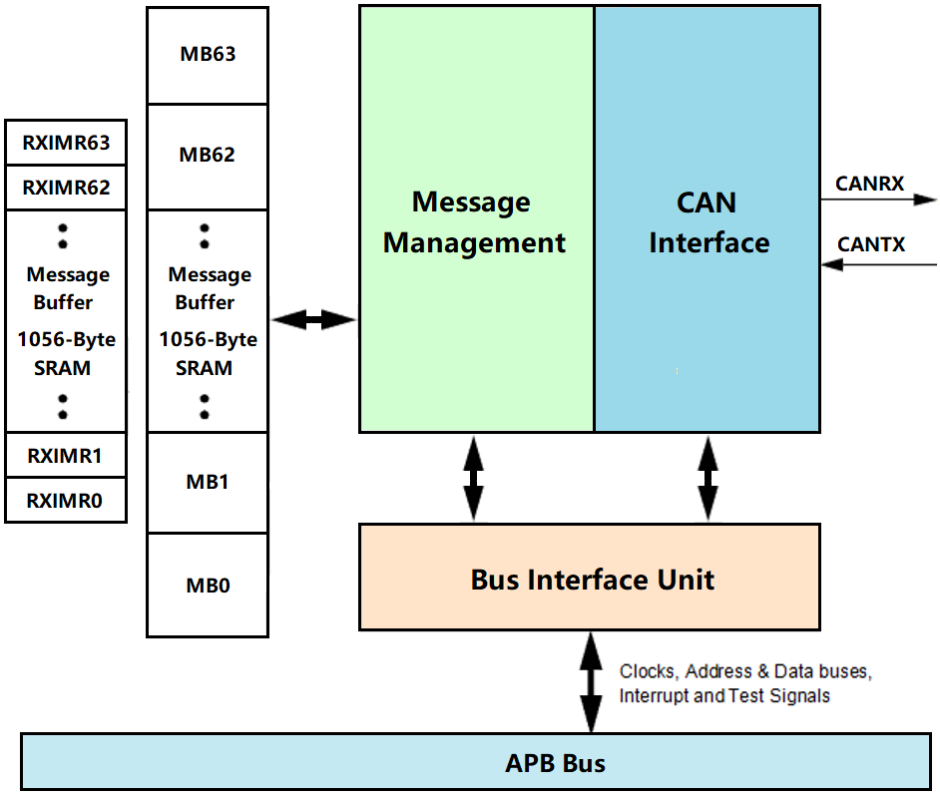


Figure 19-1: CANBus Block Diagram

19.1.1. Overview

The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. The CANBus module is a full implementation of the CAN protocol specification, version 2.0 B, which supports both standard and extended message frames.

Up to 64 Message Buffers are available. The Message Buffers are stored in an embedded SRAM dedicated to the CANBus module.

The CAN Protocol Interface (CPI) submodule manages the serial communication on the CANBus, requesting SRAM access for receiving and transmitting message frames, validating received messages and performing error handling. The Message Buffer Management (MBM) submodule handles Message Buffer selection for reception and transmission, taking care of arbitration and ID matching algorithms. The Bus Interface Unit (BIU) submodule controls the access to and from the internal interface bus, in order to establish connection to the CPU and to other blocks. Clocks, address and data buses, interrupt outputs and test signals are accessed through the Bus Interface Unit.

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19.1.2. CANBus Module Features

The CANBus module includes below distinctive features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0~8 bytes data length
  - Programmable bit rate up to 1 Mbit/s
  - Content-related addressing
- 64 Message Buffers of zero to eight bytes data length
- Each MB configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Includes 1056 bytes (64 MBs) of SRAM used for MB storage
- Includes 256 bytes (64 MBs) of SRAM used for individual Rx Mask Registers
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16 standard or 32 partial (8-bits) IDs, with individual masking capability
- Programmable clock source to the CANBUS Protocol Interface, either bus clock or crystal oscillator
- Unused MB and Rx Mask Register space can be used as general purpose SRAM space
- Listen-only mode capability
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time Stamp based on 16-bits free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode
- Hardware cancellation on Tx message buffers

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19.1.3. Modes Of Operation

The CANBus module has four functional modes: Normal Mode (User and Supervisor), Freeze Mode, Listen-Only Mode and Loop-Back Mode. There is also a low power mode: Disable Mode.

- **Normal Mode (User or Supervisor)**

  In Normal Mode, the module operates receiving and/or transmitting message frames, errors are handled normally and all the CANBUS Protocol functions are enabled. User and Supervisor Modes differ in the access to some restricted control registers.

- **Freeze Mode**

  It is enabled when the FRZ bit in the MCR is asserted. If enabled, Freeze Mode is entered when the HALT bit in MCR is set or when Debug Mode is requested at MCU level. In this mode, no transmission or reception of frames is done and synchronicity to the CANBus is lost.

- **Listen-Only Mode**

  The module enters this mode when the LOM bit in the Control Register is asserted. In this mode, transmission is disabled, all error counters are frozen and the module operates in a CANBUS Error Passive mode. Only messages acknowledged by another CAN station will be received. If CANBus detects a message that has not been acknowledged, it will flag a BIT0 error (without changing the REC), as if it was trying to acknowledge the message.

- **Loop-Back Mode**

  The module enters this mode when the LPB bit in the Control Register is asserted. In this mode, CANBus performs an internal loop back that can be used for self-test operation. The bit stream output of the transmitter is internally fed back to the receiver input. The Rx CAN input pin is ignored and the Tx CAN output goes to the recessive state (logic '1'). CANBus behaves as it normally does when transmitting and treats its own transmitted message as a message received from a remote node. In this mode, CANBus ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated.

- **Module Disable Mode**

  This Low Power Mode is entered when the MDIS bit in the MCR is asserted. When disabled, the module shuts down the clocks to the CAN Protocol Interface and Message Buffer Management submodules. Exit from this mode is done by negating the MDIS bit in the MCR.

19.2. External Signal Description

19.2.1. Overview

The CANBus module has two I/O signals connected to the external MCU pins. These signals are summarized in **Table 19-1** and described in more detail in the next subsections.

Table 19-1: CANBus Signals

Signal name	Direction	Description
CANRX	Input	CANBUS receive pin
CANTX	Output	CANBUS transmit pin

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19.2.2. Signal Descriptions

19.2.2.1. CANRX

This pin is the receive pin from the CANBus transceiver. Dominant state is represented by logic level ‘0’. Recessive state is represented by logic level ‘1’.

19.2.2.2. CANTX

This pin is the transmit pin to the CANBus transceiver. Dominant state is represented by logic level ‘0’. Recessive state is represented by logic level ‘1’.

The following is the example of Can bus application circuit.

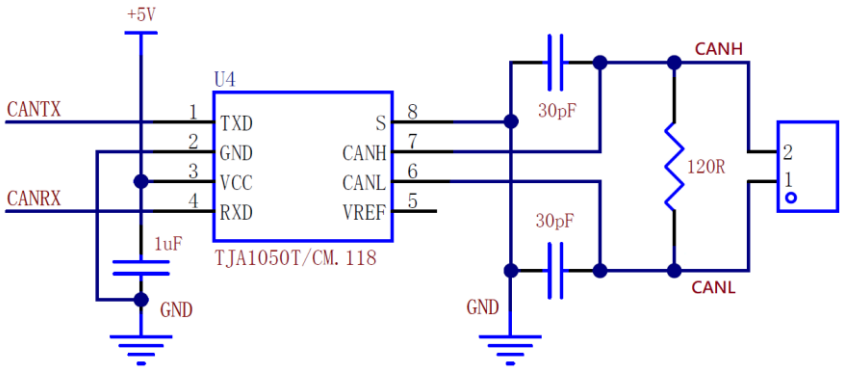


Figure 19-2: Canbus Circuit Example

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20. Serial Communication Interface (SCI)

20.1. Introduction

LT7589's Serial Communication Interface Module (SCI) supports basic UART and allows asynchronous serial communications with peripheral devices and other microcontroller units (MCU).This module also supports LIN slave operation.

20.2. Features

Features of each SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bits modulo divider) with configurable oversampling ratio from 4x to 256x
- Interrupt, polled operation:
  – Transmit data register empty and transmission complete
  – Receive data register full
  – Receive overrun, parity error, framing error, and noise error
  – Idle receiver detect
  – Active edge on receive pin
  – Break detect supporting LIN
  – Receive data match
- Hardware parity generation and checking
- Programmable 8-bits, 9-bits or 10-bits character length
- Programmable 1-bit or 2-bits stop bits
- Three receiver wakeup methods:
  – Idle line wakeup
  – Address mark wakeup
  – Receive data match
- Automatic address matching to reduce ISR overhead:
  – Address mark matching
  – Idle line address matching
  – Address match start, address match end
- Optional 13-bits break character generation / 11-bits break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- Independent FIFO structure for transmit and receive
  – Separate configurable watermark for receive and transmit requests
  – Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty

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20.3. Modes of Operation

- Stop mode
- Wait mode

20.4. Block Diagram

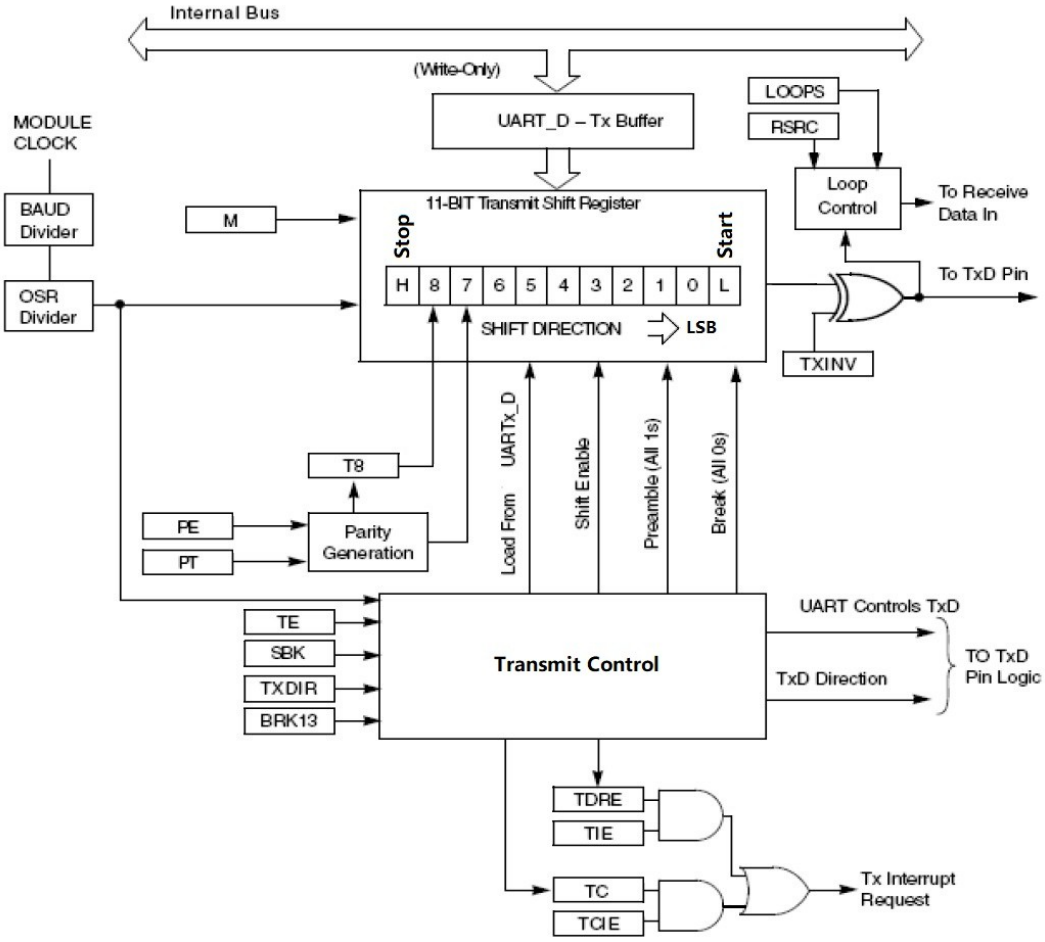


Figure 20-1: SCI Transmitter Block Diagram

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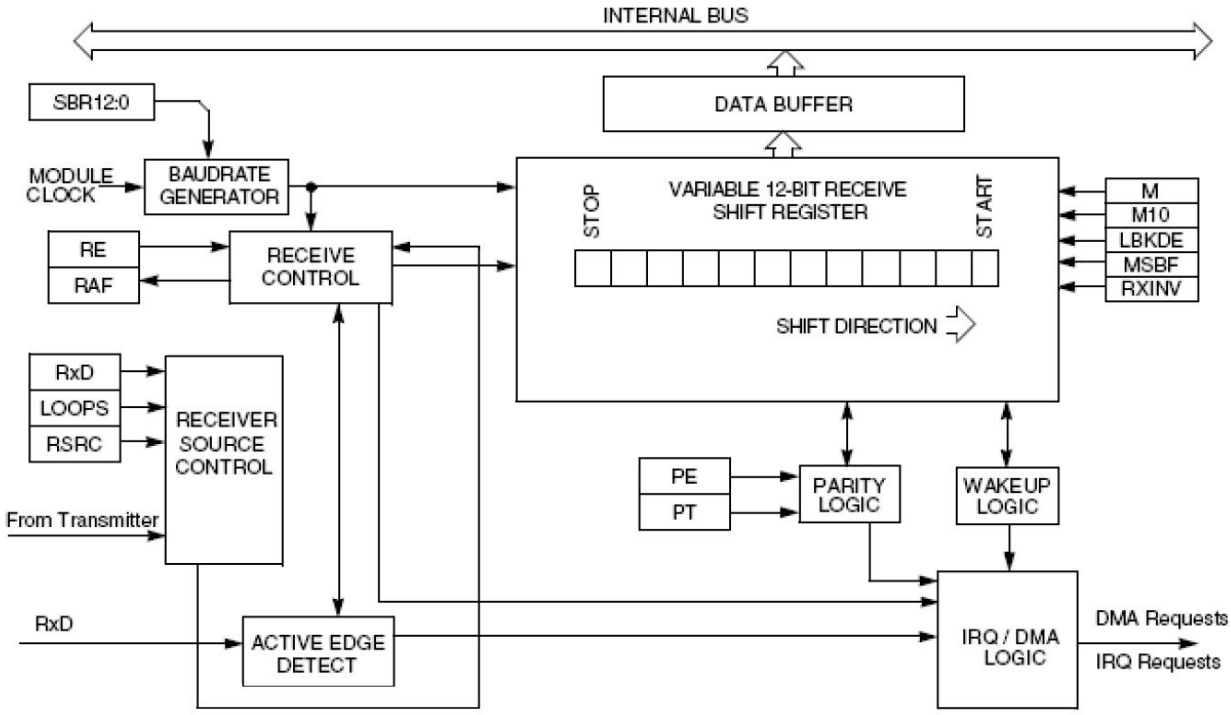


Figure 20-2: SCI Receiver Block Diagram

20.5. Modes of Operation

20.5.1. Stop Mode

The SCI will not be functional during Stop mode.

20.5.2. Wait Mode

The SCI can be configured to Stop in Wait modes, when the DOZEEN bit is set.

The transmitter and receiver will finish transmitting/receiving the current word.

20.6. Signal Description

Table 20-1 gives an overview of the signals which are described here.

Table 20-1: Signal Properties

Signal	Description	I/O
TXD	Transmit data. This pin is normally an output, but is an input (tristate) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
RXD	Receive data	I
SCI_DE	RS-485 transceiver's control signal	O

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20.7. Memory Map and Registers

20.7.1. Memory Map

The SCI Module memory map is shown in **Table 20-2**. The SCI0 base address is 0x4009_0000, SCI1 is 0x4008_0000, and SCI2 is 0x400C_0000.

Table 20-2: SCI Module Memory Map

Offset Address	Bits[31:0]
0x0000	SCI Version ID (SCI_VERID)
0x0004	SCI Parameter (SCI_PARAM)
0x0008	SCI Reset (SCI_RESET)
0x000C	SCI Pin (SCI_PIN)
0x0010	SCI Baud Rate Register (SCI_BAUD)
0x0014	SCI Status Register (SCI_STAT)
0x0018	SCI Control Register (SCI_CTRL)
0x001C	SCI Data Register (SCI_DATA)
0x0020	SCI Match Address Register (SCI_MATCH)
0x0024	SCI Modem IrDA Register (SCI_MODIR)
0x0028	SCI FIFO Register (SCI_FIFO)
0x002C	SCI Watermark Register (SCI_WATER)
0x0030	SCI Oversampling Ratio Register(SCI_OSR)

Note:

Each module is assigned 16K Bytes of address space, all of which may not be decoded. Accesses outside of the specified module memory map generate a bus error exception.

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20.7.2. Register Description

20.7.2.1. SCI Version ID Register (SCI_VERID)

Address: SCIn_BASEADDR+0x0000_0000

	31	30	29	28	27	26	25	24
Read:	VERID[31:24]							
Write:								
Reset:	0	0	0	0	0	1	0	0

	23	22	21	20	19	18	17	16
Read:	VERID[23:16]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	VERID[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	VERID[7:0]							
Write:								
Reset:	0	0	0	0	0	0	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-3: SCI Version ID Register (SCI_VERID)

VERID_ID[31:0] — SCI Version ID

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20.7.2.2. SCI Parameter Register (SCI_PARAM)

Address: SCIn_BASEADDR+0x0000_0004

	31	30	29	28	27	26	25	24
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	Reserved				RXFIFO_SZ[3:0]			
Write:								
Reset:	0	0	0	0	0	0	1	1

	7	6	5	4	3	2	1	0
Read:	Reserved				TXFIFO_SZ[3:0]			
Write:								
Reset:	0	0	0	0	0	0	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-4: SCI Parameter Register (SCI_PARAM)

RXFIFO_SZ[3:0] — The receive buffer/FIFO size
This read-only control bit indicates the the receive buffer/FIFO size.

TXFIFO_SZ[3:0] — The transmit buffer/FIFO size
This read-only control bit indicates the the transmit buffer/FIFO size.

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20.7.2.3. SCI Reset Register (SCI_RESET)

Address: SCIn_BASEADDR+0x0000_0008

	31	30	29	28	27	26	25	24
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	Reserved						SWRST	Reserved
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-5: SCI Reset Register (SCI_RESET)

SWRST — Software Reset

This read/write bit allows the software to reset SCI IP.

1 = Software reset is asserted

0 = No software reset is asserted

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20.7.2.4. SCI Pin Register (SCI_PIN)

Address: SCIn_BASEADDR+0x0000_000C

	31	30	29	28	27	26	25	24
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	Reserved						PINCFG	
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-6: SCI Pin Register (SCI_PIN)

PINCFG — Useless in this module

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20.7.2.5. SCI Baud Rate Register (SCI_BAUD)

Address: SCIn_BASEADDR+0x0000_0010

	31	30	29	28	27	26	25	24
Read:	MAEN1	MAEN2	M10	Reserved				
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	TDMAE	Reserved	RDMAE	Reserved	MATCFG[1:0]		BOTHEDG	RESYNCDIS
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	LBKDIE	RXEDGIE	SBNS	SBR[12:8]				
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	SBR[7:0]							
Write:								
Reset:	0	0	0	0	0	1	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-7: SCI Baud Rate Register (SCI_BAUD)

MAEN1 — Match Address Mode Enable 1

1 = Enable automatic address matching or data matching mode for MATCH[MA1]

0 = Normal operation

MAEN2 — Match Address Mode Enable 2

1 = Enable automatic address matching or data matching mode for MATCH[MA2]

0 = Normal operation

M10 — 10-bits Mode select

The M10 bit causes a tenth bit to be part of the serial transmission. This bit should only be changed when the transmitter and receiver are both disabled.

1 = Receiver and transmitter use 10-bits data characters

0 = Receiver and transmitter use 8-bits or 9-bits data characters

TDMAE — Transmitter DMA Enable

TDMAE configures the transmit data register empty flag, LPUART_STAT[TDRE], to generate a DMA request.

1 = DMA request is enabled

0 = DMA request is disabled

RDMAE — Receiver Full DMA Enable

RDMAE configures the receiver data register full flag, LPUART_STAT[RDRF], to generate a DMA request.

1 = DMA request is enabled

0 = DMA request is disabled

MATCFG[1:0] — Match Configuration

Configure the match addressing mode used:

00 -- Address Match Wakeup;

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01 -- Idle Match Wakeup;

10 -- Match On and Match Off;

11 -- Enable RWU on Data Match and Match On/Off for transmitter CTS input

BOTHEDGE — Both Edge Sampling

Enable sampling of the received data on both edges of the baud rate clock, effectively doubling the number of times the receiver samples the input data for a given oversampling ratio. This bit must be set for oversampling ratios between x4 and x7 and is optional for higher oversampling ratios. This bit should only be changed when the receiver is disabled.

1 = Receiver samples input data using the rising and falling edge of the baud rate clock.

0 = Receiver samples input data using the rising edge of the baud rate clock.

RESYNCDIS — Resynchronization Disable

When set, it disables the resynchronization of the received data word when a data one followed by data zero transition is detected. This bit should only be changed when the receiver is disabled.

1 = Resynchronization during received data word is disabled

0 = Resynchronization during received data word is supported

LBKDIE — LIN Break Detect Interrupt Enable

LBKDIE enables the LIN break detect flag, LBKDIF, to generate interrupt requests.

1 = Hardware interrupts are requested when SCI_STAT[LBKDIF] flag is 1

0 = Hardware interrupts from SCI_STAT[LBKDIF] are disabled (use polling)

RXEDGIE — RX Input Active Edge Interrupt Enable

Enable the receive input active edge, RXEDGIF, to generate interrupt requests. Changing CTRL[LOOP] or CTRL[RSRC] when RXEDGIE is set can cause the RXEDGIF to set.

1 = Hardware interrupt requested when SCI_STAT[RXEDGIF] flag is 1

0 = Hardware interrupts from SCI_STAT[RXEDGIF] is disabled (use polling)

SBNS — Stop Bit Number Select SBNS determines whether data characters are one or two stop bits. This bit should only be changed when the transmitter and receiver are both disabled.

1 = Two stop bits

0 = One stop bits

SBR[12:0] — Baud Rate Modulo Divisor

The 13-bits in SBR[12:0] set the modulo divide rate for the baud rate generator. When SBR is 1 - 8191, the baud rate equals "baud clock / ((OSR+1) × SBR)". The 13-bits baud rate setting [SBR12:SBR0] must only be updated when the transmitter and receiver are both disabled (SCI_CTRL[RE] and SCI_CTRL[TE] are both 0).

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20.7.2.6. SCI Status Register (SCI_STAT)

Address: SCIn_BASEADDR+0x0000_0014

	31	30	29	28	27	26	25	24
Read:	LBKDIF	RXEDGIF	MSBF	RXINV	RWUID	BRK13	LBKDE	RAF
Write:	w1c	w1c						
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Write:				w1c	w1c	w1c	w1c	w1c
Reset:	1	1	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	MA1F	MA2F	Reserved					
Write:	w1c	w1c						
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	1	0	0

= Writes have no effect and the access terminates without a transfer error exception.

w1c = .Write 1 to the bit will clear it

Figure 20-8: SCI Status Register (SCI_STAT)

LBKDIF — LIN Break Detect Interrupt Flag

LBKDIF is set when the LIN break detect circuitry is enabled and a LIN break character is detected. LBKDIF is cleared by writing a 1 to it.

1 = LIN break character has been detected

0 = No LIN break character has been detected

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RXEDGIF — RXD Pin Active Edge Interrupt Flag

RXEDGIF is set when an active edge, falling if RXINV = 0, rising if RXINV = 1, on the RXD pin occurs. RXEDGIF is cleared by writing a 1 to it.

1 = An active edge on the receive pin has occurred

0 = No active edge on the receive pin has occurred

MSBF — MSB First

Setting this bit reverses the order of the bits that are transmitted and received on the wire. This bit does not affect the polarity of the bits, the location of the parity bit or the location of the start or stop bits. This bit should only be changed when the transmitter and receiver are both disabled.

1 = MSB (bit9, bit8, bit7 or bit6) is the first bit that is transmitted following the start bit depending on the setting of CTRL[M], CTRL[PE] and BAUD[M10]. Further, the first bit received after the start bit is identified as bit9, bit8, bit7 or bit6 depending on the setting of CTRL[M] and CTRL[PE].

0 = LSB (bit0) is the first bit that is transmitted following the start bit. Further, the first bit received after the start bit is identified as bit0

RXINV — Receive Data Inversion

Setting this bit reverses the polarity of the received data input. Setting RXINV inverts the RXD input for all cases: data bits, start and stop bits, break,

and idle.

1 = Receive data are inverted

0 = Receive data are not inverted

RWUID — Receive Wake Up Idle Detect

For RWU on idle character, RWUID controls whether the idle character that wakes up the receiver sets the IDLE bit. For address match wakeup, RWUID controls if the IDLE bit is set when the address does not match. This bit should only be changed when the receiver is disabled.

1 = During receive standby state (RWU = 1), the IDLE bit gets set upon detection of an idle character. During address match wakeup, the IDLE bit does get set when an address does not match.

0 = During receive standby state (RWU = 1), the IDLE bit does not get set upon detection of an idle character. During address match wakeup, the IDLE bit does not get set when an address does not match.

BRK13 — Break Character Generation Length

BRK13 selects a longer transmitted break character length. Detection of a framing error is not affected by the state of this bit. This bit should only be changed when the transmitter is disabled.

1 = Break character is transmitted with length of 13-bits times (if M = 0, SBNS = 0) or 14 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 15 (if M = 1, SBNS = 1 or M10 = 1, SNBS = 0) or 16 (if M10 = 1, SNBS = 1).

0 = Break character is transmitted with length of 10-bits times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1 or M10 = 1, SNBS = 0) or 13 (if M10 = 1, SNBS = 1)

LBKDE — LIN Break Detection Enable

LBKDE selects a longer break character detection length. While LBKDE is set, receive data is not stored in the receive data buffer.

1 = Break character is detected at length of 11 bit times (if M = 0, SBNS = 0) or 12 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 14 (if M = 1, SBNS = 1 or M10 = 1, SNBS = 0) or 15 (if M10 = 1, SNBS = 1)

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0 = Break character is detected at length 10-bits times (if M = 0, SBNS = 0) or 11 (if M = 1, SBNS = 0 or M = 0, SBNS = 1) or 12 (if M = 1, SBNS = 1 or M10 = 1, SNBS = 0) or 13 (if M10 = 1, SNBS = 1)

RAF — Receiver Active Flag

RAF is set when the receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line.

1 = SCI receiver active (RXD input not idle)

0 = SCI receiver idle waiting for a start bit

TDRE — Transmit Data Register Empty Flag

When the transmit FIFO is enabled, TDRE will set when the number of datawords in the transmit FIFO(SCI_DATA) is equal to or less than the number indicated by SCI_WATER[TXWATER]). To clear TDRE, write to the SCI data register (SCI_DATA) until the number of words in the transmit FIFO is greater than the number indicated by SCI_WATER[TXWATER]. When the transmit FIFO is disabled, TDRE will set when the transmit data register (SCI_DATA) is empty. To clear TDRE, write to the SCI data register (SCI_DATA).

TDRE is not affected by a character that is in the process of being transmitted, it is updated at the start of each transmitted character.

1 = Transmit data buffer is empty

0 = Transmit data buffer is full

TC — Transmission Complete Flag

TC is cleared when there is a transmission in progress or when a preamble or break character is loaded. TC is set when the transmit buffer is empty and no data, preamble, or break character is being transmitted. When TC is set, the transmit data output signal becomes idle (logic 1). TC is cleared by writing to SCI_DATA to transmit new data, queuing a preamble by clearing and then setting SCI_CTRL[TE], queuing a break character by writing 1 to SCI_CTRL[SBK].

1 = Transmitter is idle (transmission activity complete)

0 = Transmitter is active (sending data, a preamble, or a break)

RDRF — Receive Data Register Full Flag

When the receive FIFO is enabled, RDRF is set when the number of datawords in the receive buffer is greater than the number indicated by SCI_WATER[RXWATER]. To clear RDRF, read SCI_DATA until the number of datawords in the receive data buffer is equal to or less than the number indicated by SCI_WATER[RXWATER]. When the receive FIFO is disabled, RDRF is set when the receive buffer (SCI_DATA) is full. To clear RDRF, read the SCI_DATA register.

A character that is in the process of being received does not cause a change in RDRF until the entire character is received. Even if RDRF is set, the character will continue to be received until an overrun condition occurs once the entire character is received.

1 = Receive data buffer is full

0 = Receive data buffer is empty

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IDLE — Idle Line Flag

IDLE is set when the SCI receive line becomes idle for a full character time after a period of activity. When ILT is cleared, the receiver starts counting idle bit times after the start bit. If the receive character is all 1s, these bit times and the stop bits time count toward the full character time of logic high, 10 to 13-bits times, needed for the receiver to detect an idle line. When ILT is set, the receiver does not start counting idle bit times until after the stop bits. The stop bits and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line.

To clear IDLE, write logic 1 to the IDLE flag. After IDLE has been cleared, it cannot become set again until after a new character has been stored in the receive buffer or a LIN break character has set the LBKDIF flag . IDLE is set only once even if the receive line remains idle for an extended period.

1 = Idle line was detected

0 = No idle line detected

OR — Receiver Overrun Flag

OR is set when software fails to prevent the receive data register from overflowing with data. The OR bit is set immediately after the stop bit has been completely received for the data word that overflows the buffer and all the other error flags (FE, NF, and PF) are prevented from setting. The data in the shift register is lost, but the data already in the SCI data registers is not affected. If LBKDE is enabled and a LIN Break is detected, the OR field asserts if LBKDIF is not cleared before the next data character is received.

While the OR flag is set, no additional data is stored in the data buffer even if sufficient room exists. To clear OR, write logic 1 to the OR flag.

1 = Receive overrun (new SCI data lost)

0 = No overrun

NF — Noise Flag

The advanced sampling technique used in the receiver takes three samples in each of the received bits. If any of these samples disagrees with the rest of the samples within any bit time in the frame then noise is detected for that character. NF is set whenever the next character to be read from SCI_DATA was received with noise detected within the character. To clear NF, write logic one to the NF.

1 = Noise detected in the received character in SCI_DATA

0 = No noise detected

FE — Framing Error Flag

FE is set whenever the next character to be read from SCI_DATA was received with logic 0 detected where a stop bit was expected. To clear FE, write logic one to the FE.

1 = Framing error

0 = No framing error detected. This does not guarantee the framing is correct

PF — Parity Error Flag

PF is set whenever the next character to be read from SCI_DATA was received when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, write a logic one to the PF.

1 = Parity error

0 = No parity error

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MA1F — Match 1 Flag

MA1F is set whenever the next character to be read from SCI_DATA matches MA1. To clear MA1F, write a logic one to the MA1F.

1 = Received data is equal to MA1

0 = Received data is not equal to MA1

MA2F — Match 2 Flag

MA2F is set whenever the next character to be read from SCI_DATA matches MA2. To clear MA2F, write a logic one to the MA2F.

1 = Received data is equal to MA2

0 = Received data is not equal to MA2

20.7.2.7. SCI Control Register (SCI_CTRL)

Address: SCIn_BASEADDR+0x0000_0018

	31	30	29	28	27	26	25	24
Read: Write:	R8T9	R9T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RUW	SBK
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read: Write:	MA1IE	MA2IE	Reserved			IDLECFG		
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: Write:	LOOPS	DOZEEN	RSRC	M	WAKE	ILT	PE	PT
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-9: SCI Control Register (SCI_CTRL)

R8T9 — Receive Bit 8 / Transmit Bit 9

R8 is the ninth data bit received when the SCI is configured for 9-bits or 10-bits data formats. When reading 9-bits or 10-bits data, read R8 before reading SCI_DATA.

T9 is the tenth data bit received when the SCI is configured for 10-bits data formats. When writing 10-bits data, write T9 before writing SCI_DATA. If T9 does not need to change from its previous value, such as when it is used to generate address mark or parity, then it need not be written each time SCI_DATA is written.

R9T8 — Receive Bit 9 / Transmit Bit 8

R9 is the tenth data bit received when the SCI is configured for 10-bits data formats. When reading 10-bits data, read R9 before reading SCI_DATA

T8 is the ninth data bit received when the SCI is configured for 9-bits or 10-bits data formats. When writing

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9-bits or 10-bits data, write T8 before writing SCI_DATA. If T8 does not need to change from its previous value, such as when it is used to generate address mark or parity, then it need not be written each time SCI_DATA is written.

TXDIR — TXD Pin Direction in Single-Wire Mode

When the SCI is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the TXD pin. When clearing TXDIR, the transmitter will finish receiving the current character (if any) before the receiver starts receiving data from the TXD pin.

1 = TXD pin is an output in single-wire mode

0 = TXD pin is an input in single-wire mode

TXINV — Transmit Data Inversion

Setting this bit reverses the polarity of the transmitted data output. Setting TXINV inverts the TXD output for all cases: data bits, start and stop bits, break, and idle.

1 = Transmit data is inverted

0 = Transmit data is not inverted

ORIE — Overrun Interrupt Enable

This bit enables the overrun flag (OR) to generate hardware interrupt requests.

1 = Hardware interrupt is requested when OR is set

0 = OR interrupts are disabled; use polling

NEIE — Noise Error Interrupt Enable

This bit enables the noise flag (NF) to generate hardware interrupt requests.

1 = Hardware interrupt is requested when NF is set

0 = NF interrupts are disabled; use polling

FEIE — Framing Error Interrupt Enable

This bit enables the framing error flag (FE) to generate hardware interrupt requests.

1 = Hardware interrupt is requested when FE is set

0 = FE interrupts are disabled; use polling

PEIE — Parity Error Interrupt Enable

This bit enables the parity error flag (PF) to generate hardware interrupt requests.

1 = Hardware interrupt is requested when PF is set

0 = PF interrupts are disabled; use polling)

TIE — Transmit Interrupt Enable

This bit enables STAT[TDRE] to generate interrupt requests.

1 = Hardware interrupt is requested when TDRE flag is 1

0 = Hardware interrupts from TDRE are disabled; use polling

TCIE — Transmission Complete Interrupt Enable for

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TCIE enables the transmission complete flag, TC, to generate interrupt requests.

1 = Hardware interrupt is requested when TC flag is 1

0 = Hardware interrupts from TC are disabled; use polling

RIE — Receiver Interrupt Enable

This bit enables STAT[RDRF] to generate interrupt requests.

1 = Hardware interrupt is requested when RDRF flag is 1

0 = Hardware interrupts from RDRF are disabled; use polling

ILIE — Idle Line Interrupt Enable

ILIE enables the idle line flag, STAT[IDLE], to generate interrupt requests.

1 = Hardware interrupt is requested when IDLE flag is 1

0 = Hardware interrupts from IDLE are disabled; use polling

TE — Transmitter Enable

This bit enables the SCI transmitter. TE can also be used to queue an idle preamble by clearing and then setting TE. When TE is cleared, this register bit will read as 1 until the transmitter has completed the current character and the TXD pin is tristate.

1 = Transmitter is enabled

0 = Transmitter is disabled

RE — Receiver Enable

This bit enables the SCI receiver. When RE is written to 0, this register bit will read as 1 until the receiver finishes receiving the current character (if any).

1 = Receiver is enabled

0 = Receiver is disabled

RWU — Receiver Wakeup Control

This field can be set to place the SCI receiver in a standby state. RWU automatically clears when an RWU event occurs, that is, an IDLE event when CTRL[WAKE] is clear or an address match when CTRL[WAKE] is set with STAT[RWUID] is clear.

RWU must be set only with CTRL[WAKE] = 0 (wakeup on idle) if the channel is currently not idle. This can be determined by STAT[RAF]. If the flag is set to wake up an IDLE event and the channel is already idle, it is possible that the SCI will discard data. This is because the data must be received or a LIN break detected after an IDLE is detected before IDLE is allowed to be reasserted.

1 = SCI receiver in standby waiting for wakeup condition

0 = Normal receiver operation

SBK — Send Break

Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 to 13, or 13 to 16 if SCI_STATBRK13] is set, bit times of logic 0 are queued as long as SBK is set. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK.

1 = Queue break character(s) to be sent

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0 = Normal transmitter operation

MA1IE — Match 1 Interrupt Enable

1 = MA1F interrupt is enabled

0 = MA1F interrupt is disabled

MA2IE — Match 2 Interrupt Enable

1 = MA2F interrupt is enabled

0 = MA2F interrupt is disabled

IDLECFG — Idle Configuration

This bit confirgures the number of idle characters that must be received before the IDLE flag is set.

000 --1 idle character;

001 -- 2 idle characters;

010 -- 4 idle characters;

011 -- 8 idle characters;

100 -- 16 idle characters;

101 -- 32 idle characters;

110 -- 64 idle characters;

111 -- 128 idle characters

LOOPS — LOOP Mode Select

When LOOPS is set, the RXD pin is disconnected from the SCI and the transmitter output is internally connected to the receiver input. The transmitter and the receiver must be enabled to use the loop function.

1 = Loop mode or single-wire mode where transmitter outputs are internally connected to receiver input (see RSRC bit)

0 = Normal operation - RXD and TXD use separate pins

DOZEEN — Doze Enable

1 = SCI is disabled in Doze mode

0 = SCI is enabled in Doze mode

RSRC — Receiver Source Select

This field has no meaning or effect unless the LOOPS field is set. When LOOPS is set, the RSRC field determines the source for the receiver shift register input.

1 = Single-wire SCI mode where the TXD pin is connected to the transmitter output and receiver input

0 = Provided LOOPS is set, RSRC is cleared, selects internal loop back mode and the SCI does not use the RXD pin

M — 9-Bit or 8-Bit Mode Select

1 = Receiver and transmitter use 9-bits data characters

0 = Receiver and transmitter use 8-bits data characters

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WAKE — Receiver Wakeup Method Select

This bit determines which condition wakes the SCI when RWU = 1: Address mark in the most significant bit position of a received data character, or An idle condition on the receive pin input signal.

1 = Configures RWU with address-mark wakeup

0 = Configures RWU for idle-line wakeup

ILT — Idle Line Type Select

This bit determines when the receiver starts counting logic 1s as idle character bits. The count begins either after a valid start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit can cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. In case the SCI is programmed with ILT = 1, a logic 0 is automatically shifted after a received stop bit, therefore resetting the idle count.

1 = Idle character bit count starts after stop bit

0 = Idle character bit count starts after start bit

PE — Parity Enable

This bit enables hardware parity generation and checking. When parity is enabled, the bit before the stop bit is immediately treated as the parity bit.

1 = Parity is enabled

0 = No hardware parity generation or checking

PT — Parity Type

Provided parity is enabled (PE = 1), this bit selects even or odd parity. Odd parity means the total number of 1s in the data character, including the parity bit, is odd. Even parity means the total number of 1s in the data character, including the parity bit, is even.

1 = Odd parity

0 = Even parity

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20.7.2.8. SCI Data Register (SCI_DATA)

Address: SCIn_BASEADDR+0x0000_001C

	31	30	29	28	27	26	25	24
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	NOISY	PARITYE	FRETSC	RXEMPT	IDLINE	Reserved	R9T9	R8T8
Write:								
Reset:	0	0	0	1	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	R7T7	R6T6	R5T5	R4T4	R3T3	R2T2	R1T1	R0T0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-10: SCI Data Register (SCI_DATA)

NOISY — The current received dataword contained in DATA[R9:R0] was received with noise

1 = The data was received with noise

0 = The dataword was received without noise

PARITYE — The current received dataword contained in DATA[R9:R0] was received with a parity error

1 = The dataword was received with a parity error

0 = The dataword was received without a parity error

FRETSC — Frame Error / Transmit Special Character

For reads, this bit indicates the current received dataword contained in DATA[R9:R0] was received with a frame error. For writes, this bit indicates a break or idle character is to be transmitted instead of the contents in DATA[T9:T0]. T9 is used to indicate a break character when 0 and an idle character when 1, the contents of DATA[T8:T0] should be zero.

1 = The dataword was received with a frame error, transmit an idle or break character on transmit

0 = The dataword was received without a frame error on read, transmit a normal character on write

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RXEMPT — Receive Buffer Empty

This bit asserts when there is no data in the receive buffer. This field does not take into account the data that is in the receive shift register.

1 = Receive buffer is empty, data returned on read is not valid

0 = Receive buffer contains valid data

IDLINE — Idle Line

This bit indicates the receiver line was idle before receiving the character in DATA[9:0]. Unlike the IDLE flag, this bit can set for the first character received when the receiver is first enabled.

1 = Receiver was idle before receiving this character

0 = Receiver was not idle before receiving this character

R9T9 — Read receive data buffer 9 or write transmit data buffer 9

R8T8 — Read receive data buffer 8 or write transmit data buffer 8

R7T7 — Read receive data buffer 7 or write transmit data buffer 7

R6T6 — Read receive data buffer 6 or write transmit data buffer 6

R5T5 — Read receive data buffer 5 or write transmit data buffer 5

R4T4 — Read receive data buffer 4 or write transmit data buffer 4

R3T3 — Read receive data buffer 3 or write transmit data buffer 3

R2T2 — Read receive data buffer 2 or write transmit data buffer 2

R1T1 — Read receive data buffer 1 or write transmit data buffer 1

R0T0 — Read receive data buffer 0 or write transmit data buffer 0

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20.7.2.9. SCI Match Address Register (SCI_MATCH)

Address: SCIn_BASEADDR+0x0000_0020

	31	30	29	28	27	26	25	24
Read:	Reserved						MA2[9:8]	
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	MA2[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	Reserved						MA1[9:8]	
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	MA1[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-11: SCI Match Address Register (SCI_MATCH)

MA2[9:0] — Match Address 2

The MA1 and MA2 registers are compared to input data addresses when the most significant bit is set and the associated BAUD[MAEN] bit is set. If a match occurs, the following data is transferred to the data register. If a match fails, the following data is discarded. Software should only write a MA register when the associated BAUD[MAEN] bit is cleared.

MA1[9:0] — Match Address 1

The MA1 and MA2 registers are compared to input data addresses when the most significant bit is set and the associated BAUD[MAEN] bit is set. If a match occurs, the following data is transferred to the data register. If a match fails, the following data is discarded. Software should only write a MA register when the associated BAUD[MAEN] bit is cleared.

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20.7.2.10. SCI Modem IrDA Register (SCI_MODIR)

Address: SCIn_BASEADDR+0x0000_0024

	31	30	29	28	27	26	25	24
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	Reserved					IREN	TNP	
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	RTSWATER							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	Reserved		TXCTSSRC	TXCTSC	RXRTSE	TXRTSPOL	TXRTSE	TXCTSE
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-12: SCI Modem IrDA Register (SCI_MODIR)

IREN — Infrared enable

This bit enables/disables the infrared modulation/demodulation.

1 = IR is enabled

0 = IR is disabled

TNP — Transmitter narrow pulse

This bit enables whether the SCI transmits a 1/OSR, 2/OSR, 3/OSR or 4/OSR narrow pulse.

00 -- 1/OSR;

01 -- 2/OSR;

10 -- 3/OSR;

11 -- 4/OSR

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RTSWATER — Receive RTS Configuration

This bit configures the point at which the RX RTS output negates, based on the number of additional characters that can be stored in the Receive FIFO. When configured to 0, RTS negates when the start bit is detected for the character that will cause the FIFO to become full.

1 = RTS asserts when the receive FIFO is less than or equal to the RXWATER configuration and negates when the receive FIFO is greater than the RXWATER configuration.

0 = RTS asserts when the receiver FIFO is full or receiving a character that causes the FIFO to become full.

TXCTSSRC — Transmit CTS Source

This bit configures the source of the CTS input.

1 = CTS input is the inverted Receiver Match result

0 = CTS input is the SCI_CTS pin

TXCTSC — Transmit CTS Configuration

This bit configures if the CTS state is checked at the start of each character or only when the transmitter is idle.

1 = CTS input is sampled when the transmitter is idle

0 = CTS input is sampled at the start of each character

RXRTSE — Receiver request-to-send enable

This bit allows the RTS output to control the CTS input of the transmitting device to prevent receiver overrun. Do not set both RXRTSE and TXRTSE.

1 = RTS is deasserted if the receiver data register is full or a start bit has been detected that would cause the receiver data register to become full. RTS is asserted if the receiver data register is not full and has not detected a start bit that would cause the receiver data register to become full. RTS assertion is configured by the RTSWATER field

0 = The receiver has no effect on RTS

TXRTSPOL — Transmitter request-to-send polarity

This bit controls the polarity of the transmitter RTS. TXRTSPOL does not affect the polarity of the receiver RTS. RTS will remain negated in the active low state unless TXRTSE is set.

1 = Transmitter RTS is active high

0 = Transmitter RTS is active low

TXRTSE — Transmitter request-to-send enable

This bit controls RTS before and after a transmission.

1 = When a character is placed into an empty transmitter data buffer, RTS asserts one bit time before the start bit is transmitted. RTS deasserts one bit time after all characters in the transmitter data buffer and shift register are completely sent, including the last stop bit

0 = The transmitter has no effect on RTS

TXCTSE — Transmitter clear-to-send enable

TXCTSE controls the operation of the transmitter. TXCTSE can be set independently from the state of TXRTSE and RXRTSE.

1 = Clear-to-send operation is enabled. The transmitter checks the state of CTS each time it is ready to send a character. If CTS is asserted, the character is sent. If CTS is deasserted, the signal TXD remains in the mark state and transmission is delayed until CTS is asserted. Changes in CTS as a character is being sent do not affect its transmission

0 = CTS has no effect on the transmitter

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20.7.2.11. SCI FIFO Register (SCI_FIFO)

Address: SCIn_BASEADDR+0x0000_0028

	31	30	29	28	27	26	25	24
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	TXEMPT	RXEMPT	Reserved				TXOF	RXUF
Write:							w1c	w1c
Reset:	1	1	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0	0	Reserved	RXIDEN[2:0]			TXOFE	RXUFE
Write:	TXFLUSH	RXFLUSH						
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	TXFE	TXFIFOSIZE[2:0]			RXFE	RXFIFOSIZE[2:0]		
Write:								
Reset:	0	0	1	0	0	0	1	0

= Writes have no effect and the access terminates without a transfer error exception.

w1c = .Write 1 to the bit will clear it

Figure 20-13: SCI FIFO Register (SCI_FIFO)

TXEMPT — Transmit Buffer/FIFO Empty

This bit asserts when there is no data in the Transmit FIFO/buffer. This field does not take into account the data that is in the transmit shift register.

1 = Transmit buffer is empty

0 = Transmit buffer is not empty

RXEMPT — Receive Buffer/FIFO Empty

This bit asserts when there is no data in the receive FIFO/Buffer. This field does not take into account the data that is in the receive shift register.

1 = Receive buffer is empty

0 = Receive buffer is not empty

TXOF — Transmitter Buffer Overflow Flag

This bit indicates that more data has been written to the transmit buffer than it can hold. This field will assert regardless of the value of TXOFE. However, an interrupt will be issued to the host only if TXOFE is set. This flag is cleared by writing a 1.

1 = At least one transmit buffer overflow has occurred since the last time the flag was cleared

0 = No transmit buffer overflow has occurred since the last time the flag was cleared

RXUF — Receiver Buffer Underflow Flag

This bit indicates that more data has been read from the receive buffer than was present. This field will assert regardless of the value of RXUFE. However, an interrupt will be issued to the host only if RXUFE is set. This flag is cleared by writing a 1.

1 = At least one receive buffer underflow has occurred since the last time the flag was cleared

0 = No receive buffer underflow has occurred since the last time the flag was cleared

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TXFLUSH — Transmit FIFO/Buffer Flush

Writing to this field causes all data that is stored in the transmit FIFO/buffer to be flushed. This does not affect the data that is in the transmit shift register.

1 = All data in the transmit FIFO/Buffer is cleared out

0 = No flush operation occurs

RXFLUSH — Receive FIFO/Buffer Flush

Writing to this field causes all data that is stored in the receive FIFO/buffer to be flushed. This does not affect the data that is in the receive shift register.

1 = All data in the receive FIFO/buffer is cleared out

0 = No flush operation occurs

RXIDEN — Receiver Idle Empty Enable

When set, it will enable the assertion of RDRF when the receiver is idle for a number of idle characters and the FIFO is not empty.

000 -- Disable RDRF assertion due to partially filled FIFO when receiver is idle;

001 -- Enable RDRF assertion due to partially filled FIFO when receiver is idle for 1 character;

010 -- Enable RDRF assertion due to partially filled FIFO when receiver is idle for 2 characters;

011 -- Enable RDRF assertion due to partially filled FIFO when receiver is idle for 4 characters;

100 -- Enable RDRF assertion due to partially filled FIFO when receiver is idle for 8 characters;

101 -- Enable RDRF assertion due to partially filled FIFO when receiver is idle for 16 characters;

110 -- Enable RDRF assertion due to partially filled FIFO when receiver is idle for 32 characters;

111 -- Enable RDRF assertion due to partially filled FIFO when receiver is idle for 64 characters.

TXOFE — Transmit FIFO Overflow Interrupt Enable

When this field is set, the TXOF flag generates an interrupt to the host.

1 = TXOF flag generates an interrupt to the host

0 = TXOF flag does not generate an interrupt to the host

RXUFE — Receive FIFO Underflow Interrupt Enable

When this field is set, the RXUF flag generates an interrupt to the host.

1 = TRXUF flag generates an interrupt to the host

0 = RXUF flag does not generate an interrupt to the host

TXFE — Transmit FIFO Enable

When this field is set, the built in FIFO structure for the transmit buffer is enabled. The size of the FIFO structure is indicated by TXFIFOSIZE. If this field is not set, the transmit buffer operates as a FIFO of depth one dataword regardless of the value in TXFIFOSIZE. Both CTRL[TE] and CTRL[RE] must be cleared prior to changing this field.

1 = Transmit FIFO is enabled. Buffer is depth indicated by TXFIFOSIZE

0 = Transmit FIFO is disabled. Buffer is depth 1. (Legacy support)

TXFIFOSIZE[2:0] — Transmit FIFO/Buffer Depth

This field indicates the maximum number of transmit datawords that can be stored in the transmit buffer. This field is read only.

000 -- Transmit FIFO/Buffer depth = 1 dataword;

001 -- Transmit FIFO/Buffer depth = 4 datawords;

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010 -- Transmit FIFO/Buffer depth = 8 datawords;
011 -- Transmit FIFO/Buffer depth = 16 datawords;
100 -- Transmit FIFO/Buffer depth = 32 datawords;
101 -- Transmit FIFO/Buffer depth = 64 datawords;
110 -- Transmit FIFO/Buffer depth = 128 datawords;
111 -- Transmit FIFO/Buffer depth = 256 datawords.

RXFE — Receive FIFO Enable

When this field is set, the built in FIFO structure for the receive buffer is enabled. The size of the FIFO structure is indicated by the RXFIFOSIZE field. If this field is not set, the receive buffer operates as a FIFO of depth one dataword regardless of the value in RXFIFOSIZE. Both CTRL[TE] and CTRL[RE] must be cleared prior to changing this field.

1 = Receive FIFO is enabled. Buffer is the depth indicated by RXFIFOSIZE
0 = Receive FIFO is disabled. Buffer is depth 1. (Legacy support)

RXFIFOSIZE[2:0] — Receive FIFO/Buffer Depth

The maximum number of transmit datawords that can be stored in the receive buffer. This field is read only.

000 -- Receive FIFO/Buffer depth = 1 dataword;
001 -- Receive FIFO/Buffer depth = 4 datawords;
010 -- Receive FIFO/Buffer depth = 8 datawords;
011 -- Receive FIFO/Buffer depth = 16 datawords;
100 -- Receive FIFO/Buffer depth = 32 datawords;
101 -- Receive FIFO/Buffer depth = 64 datawords;
110 -- Receive FIFO/Buffer depth = 128 datawords;
111 -- Receive FIFO/Buffer depth = 256 datawords;

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20.7.2.12. SCI Watermark Register (SCI_WATER)

Address: SCIn_BASEADDR+0x0000_002C

	31	30	29	28	27	26	25	24
Read:	RXCOUNT[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	RXWATER[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	TXCOUNT[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	TXWATER[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-14: SCI Watermark Register (SCI_WATER)

RXCOUNT[7:0] — Receive Counter

The value in this register indicates the number of datawords that are in the receive FIFO/buffer. If a dataword is being received, that is, in the receive shift register, it is not included in the count. This value may be used in conjunction with FIFO[RXFIFOSIZE] to calculate how much room is left in the receive FIFO/buffer.

RXWATER[7:0] — Receive Watermark

When the number of datawords in the receive FIFO/buffer is greater than the value in this register field, an interrupt is generated. For proper operation, the value in RXWATER must be set to be less than the receive FIFO/buffer size as indicated by FIFO[RXFIFOSIZE] and FIFO[RXFE] and must be greater than 0.

TXCOUNT[7:0] — Transmit Counter

The value in this register indicates the number of datawords that are in the transmit FIFO/buffer. If a dataword is being transmitted, that is, in the transmit shift register, it is not included in the count. This value may be used in conjunction with FIFO[TXFIFOSIZE] to calculate how much room is left in the transmit FIFO/buffer.

TXWATER[7:0] — Transmit Watermark

When the number of datawords in the transmit FIFO/buffer is equal to or less than the value in this register field, an interrupt is generated. For proper operation, the value in TXWATER must be set to be less than the size of the transmit buffer/FIFO size as indicated by FIFO[TXFIFOSIZE] and FIFO[TXFE].

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20.7.2.13. SCI Oversampling Ratio Register (SCI_OSR)

Address: SCIn_BASEADDR+0x0000_0030

	31	30	29	28	27	26	25	24
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	Reserved							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	OSR[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 20-15: SCI Oversampling Ratio Register (SCI_OSR)

OSR[7:0] — Oversampling Ratio

This field configures the oversampling ratio for the receiver between 4x (00000011) and 256x (11111111). Writing an invalid oversampling ratio (for example, a value not between 4x and 256x) will default to an oversampling ratio of 16 (00001111). The OSR field should only be changed when the transmitter and receiver are both disabled. The oversampling ratio = OSR + 1.

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20.8. Functional Description

The SCI supports full-duplex, asynchronous, and NRZ serial communication, and comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. The following describes each of the blocks of the SCI.

20.9. Baud Rate Generation

A 13-bits modulus counter in the baud rate generator derive the baud rate for both the receiver and the transmitter. The value from 1 to 8191 written to SBR[12:0] determines the baud clock divisor for the asynchronous SCI baud clock. The SBR bits are in the SCI baud rate registers, BDH and BDL. The baud rate clock drives the receiver, while the transmitter is driven by the baud rate clock divided by the over sampling ratio. Depending on the over sampling ratio, the receiver has an acquisition rate of 4 to 256 samples per bit time.

Baud rate generation is subject to two sources of error:

- Integer division of the asynchronous SCI baud clock may not give the exact target frequency.
- Synchronization with the asynchronous SCI baud clock can cause phase shift

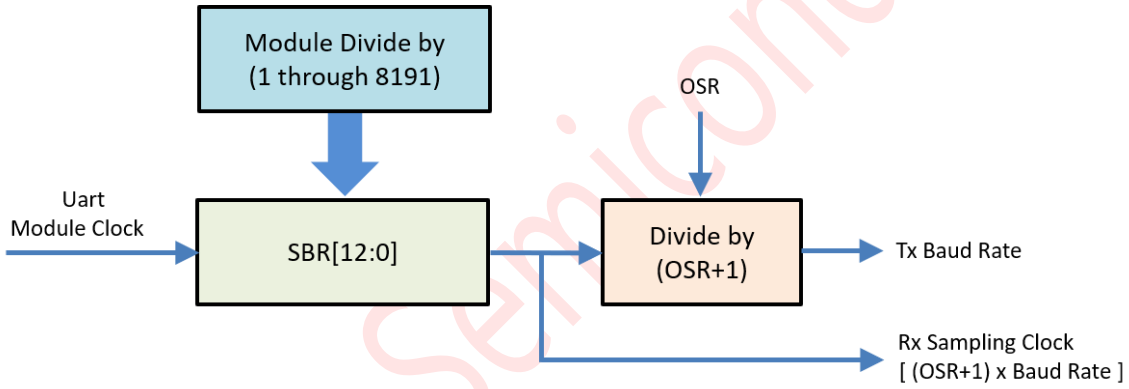


Figure 20-16: SCI Baud Rate Generation

$$\text{Baud Rate} = \frac{\text{Uart Module Clock}}{\text{SBR[12:0]} \times (\text{OSR+1})}$$

Note: Baud Rate Generator off if SBR[12:0] = 0.

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20.10. Transmitter Functional Description

This section describes the overall block diagram for the SCI transmitter, as well as specialized functions for sending break and idle characters.

The transmitter output (TXD) idle state defaults to logic high, CTRL[TXINV] is cleared following reset. The transmitter output is inverted by setting CTRL[TXINV]. The transmitter is enabled by setting the CTRL[TE] bit. This queues a preamble character that is one full character frame of the idle state. The transmitter then remains idle until data is available in the transmit data buffer. Programs store data into the transmit data buffer by writing to the SCI data register.

The central element of the SCI transmitter is the transmit shift register that is 10-bits to 13-bits long depending on the setting in the CTRL[M], BAUD[M10] and BAUD[SBNS] control bits. For the remainder of this section, assume CTRL[M], BAUD[M10] and BAUD[SBNS] are cleared, selecting the normal 8-bits data mode. In 8-bits data mode, the shift register holds a start bit, eight data bits, and a stop bit. When the transmit shift register is available for a new character, the value waiting in the transmit data register is transferred to the shift register, synchronized with the baud rate clock, and the transmit data register empty (STAT[TDRE]) status flag is set to indicate another character may be written to the transmit data buffer at SCI_DATA.

If no new character is waiting in the transmit data buffer after a stop bit is shifted out the TXD pin, the transmitter sets the transmit complete flag and enters an idle mode, with TXD high, waiting for more characters to transmit.

Writing 0 to CTRL[TE] does not immediately disable the transmitter. The current transmit activity in progress must first be completed (that could include a data character, idle character or break character), although the transmitter will not start transmitting another character.

20.10.1. Send Break And Queued Idle

The SCI_CTRL[SBK] bit sends break characters originally used to gain the attention of old teletype receivers. Break characters are a full character time of logic 0,10-bits to 12-bits times including the start and stop bits. A longer break of 13-bits times can be enabled by setting SCI_STAT[BRK13]. Normally, a program would wait for SCI_STAT[TDRE] to become set to indicate the last character of a message has moved to the transmit shifter, write 1, and then write 0 to the SCI_CTRL[SBK] bit. This action queues a break character to be sent as soon as the shifter is available. If SCI_CTRL[SBK] remains 1 when the queued break moves into the shifter, synchronized to the baud rate clock, an additional break character is queued. If the receiving device is another Freescale Semiconductor SCI, the break characters are received as 0s in all data bits and a framing error (SCI_STAT[FE] = 1) occurs.

A break character can also be transmitted by writing to the SCI_DATA register with bit 13 set and the data bits cleared. This supports transmitting the break character as part of the normal data stream.

When idle-line wakeup is used, a full character time of idle (logic 1) is needed between messages to wake up any sleeping receivers. Normally, a program would wait for SCI_STAT[TDRE] to become set to indicate the last character of a message has moved to the transmit shifter, then write 0 and then write 1 to the SCI_CTRL[TE] bit. This action queues an idle character to be sent as soon as the shifter is available. As long as the character in the shifter is not finished while SCI_CTRL[TE] is cleared, the SCI transmitter never actually releases control of the TXD pin.

An idle character can also be transmitted by writing to the SCI_DATA register with bit 13 set and the data bits also set. This supports transmitting the idle character as part of the normal data stream.

The length of the break character is affected by the SCI_STAT[BRK13], SCI_CTRL[M], SCI_BAUD[M10], and SCI_BAUD[SNBS] bits as shown below.

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Table 20-3: Break Character Length

BRK13	M	M10	SBNS	Break Character Length
0	0	0	0	10-bits times
0	0	0	1	11-bits times
0	1	0	0	11-bits times
0	1	0	1	12-bits times
0	X	1	0	12-bits times
0	X	1	1	13-bits times
1	0	0	0	13-bits times
1	0	0	1	13-bits times
1	1	0	0	14-bits times
1	1	0	1	14-bits times
1	X	1	0	15-bits times
1	X	1	1	15-bits times

20.11. Receiver Functional Description

In this section, the receiver block diagram is a guide for the overall receiver functional description. Next, the data sampling technique used to reconstruct receiver data is described in more detail. Finally, different variations of the receiver wakeup function are explained.

The receiver input is inverted by setting SCI_STAT[RXINV]. The receiver is enabled by setting the SCI_CTRL[RE] bit. Character frames consist of a start bit of logic 0, eight to ten data bits (MSB or LSB first), and one or two stop bits of logic 1. For information about 9-bits or 10-bits data mode, refer to 8-bits, 9-bits and 10-bits data modes. For the remainder of this discussion, assume the SCI is configured for normal 8-bits data mode.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (SCI_STAT[RDRF]) status flag is set. If SCI_STAT[RDRF] has already been set, it indicates the receive data register (buffer) has already been full, the overrun (OR) status flag is set and the new data is lost. Because the SCI receiver is double-buffered, the program has one full character time after SCI_STAT[RDRF] is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects that the receive data register is full (SCI_STAT[RDRF] = 1), it gets the data from the receive data register by reading SCI_DATA. Refer to Interrupts and status flags for details about flag clearing.

20.11.1. Data Sampling Technique

The SCI receiver supports a configurable oversampling rate of between 4× and 256× of the baud rate clock for sampling. The receiver starts by taking logic level samples at the oversampling rate times the baud rate to search for a falling edge on the RXD serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The oversampling baud rate clock divides the bit time into 4 to 256 segments from 1 to OSR (where OSR is the configured oversampling ratio). When a falling edge is located, three more samples are taken at (OSR/2), (OSR/2)+1, and (OSR/2)+2 to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a received character. If another falling edge is detected before the receiver is considered synchronized, the receiver restarts the sampling from the first segment.

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The receiver then samples each bit time, including the start and stop bits, at (OSR/2), (OSR/2)+1, and (OSR/2)+2 to determine the logic level for that bit. The logic level is interpreted to be that of the majority of the samples taken during the bit time. If any sample in any bit time, including the start and stop bits, in a character frame fails to agree with the logic level for that bit, the noise flag (SCI_STAT[NF]) is set when the received character is transferred to the receive data buffer.

When the SCI receiver is configured to sample on both edges of the baud rate clock, the number of segments in each received bit is effectively doubled (from 1 to OSR×2). The start and data bits are then sampled at OSR, OSR+1 and OSR+2. Sampling on both edges of the clock must be enabled for oversampling rates of 4× to 7× and is optional for higher oversampling rates.

The falling edge detection logic continuously looks for falling edges. If an edge is detected, the sample clock is resynchronized to bit times (unless resynchronization has been disabled). This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, if the received character was not a break character, the sampling logic that searches for a falling edge is filled with three logic 1 samples so that a new start bit can be detected almost immediately.

20.11.2. Receiver Wakeup Operation

Receiver wakeup and receiver address matching is a hardware mechanism that allows an SCI receiver to ignore the characters in a message intended for a different receiver.

During receiver wakeup, all receivers evaluate the first character(s) of each message, and as soon as they determine the message is intended for a different receiver, they write logic 1 to the receiver wake up control bit (SCI_CTRL[RWU]). When RWU bit and SCI_S2[RWUID] bit are set, the status flags associated with the receiver, with the exception of the idle bit, IDLE, are inhibited from setting, thus eliminating the software overhead for handling the unimportant message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force SCI_CTRL[RWU] to 0 so all receivers wake up in time to look at the first character(s) of the next message.

During receiver address matching, the address matching is performed in hardware and the SCI receiver will ignore all characters that do not meet the address match requirements.

The Receiver Wakeup is affected by the SCI_CTRL[RWU], SCI_MATCH [MA1], SCI_MATCH [MA2], SCI_BAUD[MATCFG], and SCI_STAT[RWUID] bits as shown below.

Table 20-4: Receiver Wakeup Options

RWU	MA1 | MA2	MATCFG	WAKE: RWUID	Receiver Wakeup
0	0	X	X	Normal operation
1	0	00	00	Receiver wakeup on idle line, IDLE flag not set
1	0	00	01	Receiver wakeup on idle line, IDLE flag set
1	0	00	10	Receiver wakeup on address mark
1	1	11	X0	Receiver wakeup on data match
0	1	00	X0	Address mark address match, IDLE flag not set for discarded characters

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0	1	00	X1	Address mark address match, IDLE flag set for discarded characters
0	1	01	X0	Idle line address match
0	1	10	X0	Address match on and address match off, IDLE flag not set for discarded characters
0	1	10	X1	Address match on and address match off, IDLE flag set for discarded characters

20.11.2.1. Idle-line Wakeup

When wake is cleared, the receiver is configured for idle-line wakeup. In this mode, SCI_CTRL[RWU] is cleared automatically when the receiver detects a full character time of the idle-line level. The SCI_CTRL[M] and SCI_BAUD[M10] control bit selects 8-bits to 10-bits data mode and the SCI_BAUD[SBNS] bit selects 1-bit or 2-bits stop bit number that determines how many bit times of idle are needed to constitute a full character time, 10 to 13-bits times because of the start and stop bits.

When SCI_CTRL[RWU] is one and SCI_STAT[RWUID] is zero, the idle condition that wakes up the receiver does not set the SCI_STAT[IDLE] flag. The receiver wakes up and waits for the first data character of the next message that sets the SCI_STAT[RDRF] flag and generates an interrupt if enabled. When SCI_STAT[RWUID] is one, any idle condition sets the SCI_STAT[IDLE] flag and generates an interrupt if enabled, regardless of whether SCI_CTRL[RWU] is zero or one.

The idle-line type (SCI_CTRL[ILT]) control bit selects one of two ways to detect an idle line. When SCI_CTRL[ILT] is cleared, the idle bit counter starts after the start bit so the stop bit and any logic 1s at the end of a character count toward the full character time of idle. When SCI_CTRL[ILT] is set, the idle bit counter does not start until after the stop bit time, so the idle detection is not affected by the data in the last character of the previous message.

20.11.2.2. Address-mark Wakeup

When SCI_CTRL[WAKE] is set, the receiver is configured for address-mark wakeup. In this mode, SCI_CTRL[RWU] is cleared automatically when the receiver detects a logic 1 in the most significant bit of a received character.

Address-mark wakeup allows messages to contain idle characters, but requires the MSB be reserved for use in address frames. The logic 1 in the MSB of an address frame clears the SCI_CTRL[RWU] bit before the stop bits are received and sets the SCI_STAT[RDRF] flag. In this case, the character with the MSB set is received even though the receiver was sleeping during most of this character time.

20.11.2.3. Data Match Wakeup

When SCI_CTRL[RWU] is set and SCI_BAUD[MATCFG] equals 11, the receiver is configured for data match wakeup. In this mode, SCI_CTRL[RWU] is cleared automatically when the receiver detects a character that matches MATCH[MA1] field when BAUD[MAEN1] is set, or that matches MATCH[MA2] when BAUD[MAEN2] is set.

20.11.2.4. Address Match Operation

Address match operation is enabled when the SCI_BAUD[MAEN1] or SCI_BAUD[MAEN2] bit is set and SCI_BAUD[MATCFG] is equal to 00. In this function, a character received by the RXD pin with a logic 1 in the bit position immediately preceding the stop bit is considered an address and is compared with the associated MATCH[MA1] or MATCH[MA2] field. The character is only transferred to the receive buffer, and SCI_STAT[RDRF] is set, if the comparison matches. All subsequent characters received with a logic 0 in the

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bit position immediately preceding the stop bit are considered to be data associated with the address and are transferred to the receive data buffer. If no marked address match occurs then no transfer is made to the receive data buffer, and all following characters with logic zero in the bit position immediately preceding the stop bit are also discarded. If both the SCI_BAUD[MAEN1] and SCI_BAUD[MAEN2] bits are negated, the receiver operates normally and all data received is transferred to the receive data buffer.

Address match operation functions in the same way for both MATCH[MA1] and MATCH[MA2] fields.

- If only one of SCI_BAUD[MAEN1] and SCI_BAUD[MAEN2] is asserted, a marked address is compared only with the associated match register and data is transferred to the receive data buffer only on a match.

- If SCI_BAUD[MAEN1] and SCI_BAUD[MAEN2] are asserted, a marked address is compared with both match registers and data is transferred only on a match with either register.

20.11.2.5. Idle Match Operation

Idle match operation is enabled when the SCI_BAUD[MAEN1] or SCI_BAUD[MAEN2] bit is set and SCI _BAUD[MATCFG] is equal to 01. In this function, the first character received by the RXD pin after an idle line condition is considered an address and is compared with the associated MA1 or MA2 register. The character is only transferred to the receive buffer, and SCI_STAT[RDRF] is set, if the comparison matches. All subsequent characters are considered to be data associated with the address and are transferred to the receive data buffer until the next idle line condition is detected. If no address match occurs then no transfer is made to the receive data buffer, and all following frames until the next idle condition are also discarded. If both the SCI_BAUD[MAEN1] and SCI_BAUD[MAEN2] bits are negated, the receiver operates normally and all data received is transferred to the receive data buffer.
Idle match operation functions in the same way for both MA1 and MA2 registers.

- If only one of SCI_BAUD[MAEN1] and SCI_BAUD[MAEN2] is asserted, the first character after an idle line is compared only with the associated match register and data is transferred to the receive data buffer only on a match.

- If SCI_BAUD[MAEN1] and SCI_BAUD[MAEN2] are asserted, the first character after an idle line is compared with both match registers and data is transferred only on a match with either register.

20.11.2.6. Match On Match Off Operation

Match on, match off operation is enabled when both SCI_BAUD[MAEN1] and SCI_BAUD[MAEN2] are set and SCI_BAUD[MATCFG] is equal to 10. In this function, a character received by the RXD pin that matches MATCH[MA1] is received and transferred to the receive buffer, and SCI_STAT[RDRF] is set. All subsequent characters are considered to be data and are also transferred to the receive data buffer, until a character is received that matches MATCH[MA2] register. The character that matches MATCH[MA2] and all following characters are discarded, this continues until another character that matches MATCH[MA1] is received. If both the SCI_BAUD[MAEN1] and SCI_BAUD[MAEN2] bits are negated, the receiver operates normally and all data received is transferred to the receive data buffer.

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20.11.3. Infrared Decoder

The infrared decoder converts the received character from the IrDA format to the NRZ format used by the receiver. It also has a OSR oversampling baud rate clock counter that filters noise and indicates when a 1 is received.

20.11.3.1. Start Bit Detection

When STAT[RXINV] is cleared, the first falling edge of the received character corresponds to the start bit. The infrared decoder resets its counter. At this time, the receiver also begins its start bit detection process. After the start bit is detected, the receiver synchronizes its bit times to this start bit time. For the rest of the character reception, the infrared decoder's counter and the receiver's bit time counter count independently from each other.

20.11.3.2. Noise Filtering

Any further rising edges detected during the first half of the infrared decoder counter are ignored by the decoder. Any pulses less than one oversampling baud clock can be undetected by it regardless of whether it is seen in the first or second half of the count.

20.11.3.3. Lowbits Detection

During the second half of the decoder count, a rising edge is decoded as a 0, which is sent to the receiver. The decoder counter is also reset.

20.11.3.4. Highbits Detection

At OSR oversampling baud rate clocks after the previous rising edge, if a rising edge is not seen, then the decoder sends a 1 to the receiver.

If the next bit is a 0, which arrives late, then a lowbits is detected according to Lowbits detection. The value sent to the receiver is changed from 1 to a 0. Then, if a noise pulse occurs outside the receiver's bit time sampling period, then the delay of a 0 is not recorded as noise.

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20.12. Additional SCI Functions

The following sections describe additional SCI functions.

20.12.1. 8-bits, 9-bits and 10-bits Data Modes

The SCI transmitter and receiver can be configured to operate in 9-bits data mode by setting the SCI_ CTRL[M] or 10-bits data mode by setting SCI_BAUD[M10]. In 9-bits mode, there is a ninth data bit, and in 10-bits mode, there is a tenth data bit. For the transmit data buffer, these bits are stored in SCI_CTRL[T8] and SCI_CTRL[T9]. For the receiver, these bits are held in SCI_CTRL[R8] and SCI_CTRL[R9]. They are also accessible via 16-bits or 32-bits accesses to the SCI_DATA register.
For coherent 8-bits writes to the transmit data buffer, write to SCI_CTRL[T8] and SCI_CTRL[T9] before writing to SCI_DATA[7:0]. For 16-bits and 32-bits writes to the SCI_DATA register, all 10 transmit bits are written to the transmit data buffer at the same time.

If the bit values to be transmitted as the ninth and tenth bit of a new character are the same as those of the previous character, it is not necessary to write to SCI_CTRL[T8] and SCI_CTRL[T9] again. When data is transferred from the transmit data buffer to the transmit shifter, the value in SCI_CTRL[T8] and SCI_CTRL[T9] is copied at the same time data is transferred from SCI_DATA[7:0] to the shifter.

The 9-bits data mode is typically used with parity to allow eight bits of data plus the parity in the ninth bit, or it is used with address-mark wakeup so the ninth data bit can serve as the wakeup bit. The 10-bits data mode is typically used with parity and address-mark wakeup so the ninth data bit can serve as the wakeup bit and the tenth bit as the parity bit. In custom protocols, the ninth and/or tenth bits can also serve as software-controlled markers.

20.12.2. Idle Length

An idle character is a character where the start bit, all data bits and stop bits are in the mark position. The CTRL[ILT] register can be configured to start detecting an idle character from the previous start bit (any data bits and stop bits count towards the idle character detection) or from the previous stop bit.

The number of idle characters that must be received before an idle line condition is detected can also be configured using the CTRL[IDLECFG] field. This field configures the number of idle characters that must be received before the STAT[IDLE] flag is set, the STAT[RAF] flag is cleared and the DATA[IDLINE] flag is set with the next received character.

Idle-line wakeup and idle match operation are also affected by the CTRL[IDLECFG] field. When address match or match on/off operation is enabled, setting the STAT[RWUID] bit will cause any discarded characters to be treated as if they were idle characters. independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the RXD pin is not used by the SCI.

20.12.3. Single-wire Operation

When SCI_CTRL[LOOPS] is set, the SCI_CTRL[RSRC] bit in the same register chooses between loop mode (SCI_CTRL[RSRC] = 0) or single-wire mode (SCI_CTRL[RSRC] = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the RXD pin is not used by the SCI.

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20.12.4. Loop Mode

When SCI_CTRL[LOOPS] is set, the RSRC bit in the same register chooses between loop mode (SCI_CTRL[RSRC] = 0) or single-wire mode (SCI_CTRL[RSRC] = 1). Single-wire mode implements a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TXD pin (the RXD pin is not used).

In single-wire mode, the SCI_CTRL[TXDIR] bit controls the direction of serial data on the TXD pin. When SCI_CTRL[TXDIR] is cleared, the TXD pin is an input to the receiver and the transmitter is temporarily disconnected from the TXD pin so an external device can send serial data to the receiver. When SCI_CTRL[TXDIR] is set, the TXD pin is an output driven by the transmitter, the internal loop back connection is disabled, and as a result, the receiver cannot receive characters that are sent out by the transmitter.

20.13. Infrared Interface

The SCI provides the capability of transmitting narrow pulses to an IR LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI. The IrDA physical layer specification defines a half-duplex infrared communication link for exchanging data. The full standard includes data rates up to 16 Mbits/s. This design covers data rates only between 2.4 kbits/s and 115.2 kbits/s.

The SCI has an infrared transmit encoder and receive decoder. The SCI transmits serial bits of data that are encoded by the infrared submodule to transmit a narrow pulse for every zero bit. No pulse is transmitted for every one bit. When receiving data, the IR pulses are detected using an IR photo diode and transformed to CMOS levels by the IR receive decoder, external from the SCI. The narrow pulses are then stretched by the infrared receive decoder to get back to a serial bit stream to be received by the UART. The polarity of transmitted pulses and expected receive pulses can be inverted so that a direct connection can be made to external IrDA transceiver modules that use active high pulses.

The infrared submodule receives its clock sources from the SCI. One of these two clocks are selected in the infrared submodule to generate either 1/OSR, 2/OSR, 3/OSR, or 4/OSR narrow pulses during transmission.

20.13.1. Infrared Transmit Encoder

The infrared transmit encoder converts serial bits of data from transmit shift register to the TXD signal. A narrow pulse is transmitted for a zero bit and no pulse for a one bit. The narrow pulse is sent at the start of the bit with a duration of 1/OSR, 2/OSR, 3/OSR, or 4/OSR of a bit time. A narrow low pulse is transmitted for a zero bit when SCI_CTRL[TXINV] is cleared, while a narrow high pulse is transmitted for a zero bit when SCI_CTRL[TXINV] is set.

20.13.2. Infrared Receive Decoder

The infrared receive block converts data from the RXD signal to the receive shift register. A narrow pulse is expected for each zero received and no pulse is expected for each one received. A narrow low pulse is expected for a zero bit when SCI_STAT[RXINV] is cleared, while a narrow high pulse is expected for a zero bit when SCI_STAT[RXINV] is set. This receive decoder meets the edge jitter requirement as defined by the IrDA serial infrared physical layer specification.

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20.14. Interrupts And Status Flags

The SCI transmitter has two status flags that can optionally generate hardware interrupt requests. The transmit data register empty SCI_(STAT[TDRE]) bit indicates when there is room in the transmit data buffer to write another transmit character to SCI_DATA. If the transmit interrupt enable SCI_CTRL[TIE]) bit is set, a hardware interrupt is requested when SCI_STAT[TDRE] is set. The transmit complete (SCI_STAT[TC]) bit indicates that the transmitter is finished transmitting all data, preamble, and break characters and is idle with TXD at the inactive level. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (SCI_CTRL[TCIE]) bit is set, a hardware interrupt is requested when SCI_STAT[TC] is set. Instead of hardware interrupts, software polling may be used to monitor the SCI_STAT[TDRE] and SCI_STAT[TC] status flags if the corresponding SCI_CTRL[TIE] or SCI_CTRL[TCIE] local interrupt masks are cleared.

When a program detects that the receive data register is full (SCI_STAT[RDRF] = 1), it gets the data from the receive data register by reading SCI_DATA. The SCI_STAT[RDRF] flag is cleared by reading SCI_DATA.

The IDLE status flag includes logic that prevents it from getting set repeatedly when the RXD line remains idle for an extended period of time. IDLE is cleared by writing 1 to the SCI _STAT[IDLE] flag. After SCI_STAT[IDLE] has been cleared, it cannot become set again until the receiver has received at least one new character and has set SCI_STAT[RDRF].

If the associated error was detected in the received character that caused SCI_STAT[RDRF] to be set, the error flags - noise flag (SCI_STAT[NF]), framing error (SCI_STAT[FE]), and parity error flag (SCI_STAT[PF]) - are set at the same time as SCI_STAT[RDRF]. These flags are not set in overrun cases.

If SCI_STAT[RDRF] was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (SCI_STAT[OR]) flag is set instead of the data along with any associated NF, FE, or PF condition is lost.

If the received character matches the contents of MATCH[MA1] and/or MATCH[MA2] then the SCI_STAT[MA1F] and/or SCI_STAT[MA2F] flags are set at the same time that SCI_STAT[RDRF] is set.

At any time, an active edge on the RXD serial data input pin causes the SCI_STAT[RXEDGIF] flag to set. The SCI_STAT[RXEDGIF] flag is cleared by writing a 1 to it. This function depends on the receiver being enabled (SCI_CTRL[RE] = 1).

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21. Synchronous Serial Interface (SSI)

21.1. Introduction

SSI is a programmable Synchronous Serial Interface (SSI) peripheral. This is an AMBA 2.0-compliant AHB (Advanced High-performance Bus) component .The host processor accesses data, control, and status information on the SSI through the AHB interface. The SSI may also interface with a DMA Controller using an optional set of DMA signals, which can be selected during configuration.

LT7589's SSI module provides QSPI0, QSPI1 and QSPI2 interface to SPI Flash or other SPI devices. The QSPI0 signals are connected directly to the embedded SPI Flash memory, and the QSPI1 and QSPI2 signals are available for users.

21.2. Features

Feathers include:

- Serial-master Operation.
- DMA Controller Interface – This enables the SSI to interface to a DMA controller over the bus using handshaking interface for transfer requests.
- Clock stretching support in enhanced SPI transfers.
- Data item size (4 to 32-bits) – Item size of each data transfer under control of the programmer.
- FIFO Depth – The transmit and receive FIFO buffers are 8 words deep. The FIFO width is fixed at 32-bits.
- Enhanced SPI Support.
- Execute in Place (XIP) Mode Support.

21.3. Modes of Operation

The SSI functions in these three modes:

1. Run Mode — Run mode is the normal mode of operation.
2. Doze Mode — Doze mode is a configurable low-power mode.
3. Stop Mode — The SSI is inactive in stop mode.

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21.4. Block Diagram

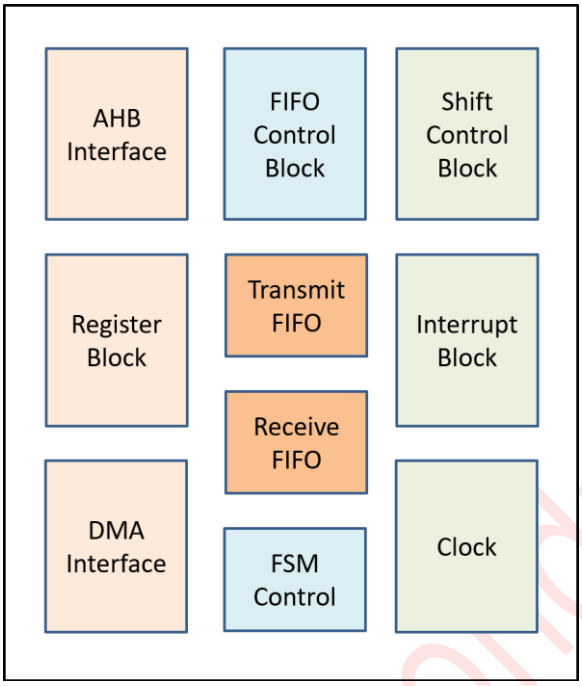


Figure 21-1: SSI Block Diagram

21.5. Application Diagram

The following is the application of LT7589's SSI module.

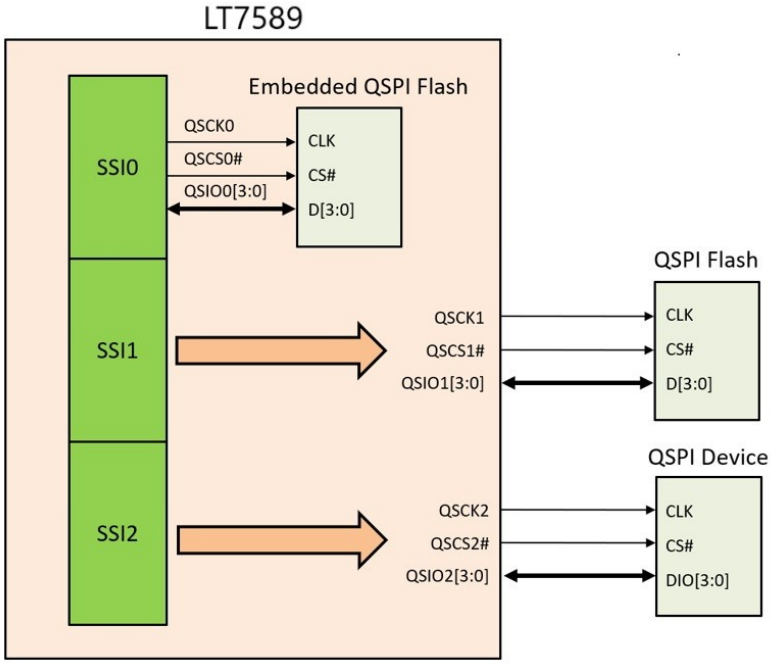


Figure 21-2: SSI Application Diagram

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21.6. Memory Map and Registers

21.6.1. Memory Map

The SSI Module memory map is shown in **Table 21-1.** The QSPI0 base address is 0x6000_0000, and QSPI1 is 0x7000_0000, and QSPI2 is 0x8000_0000.

Table 21-1: SSI Memory Map

Offset Address	Bits[31:0]	Access
0x0000	Control Register 0 (CTRLR0)	S/U
0x0004	Control Register 1 (CTRLR1)	S/U
0x0008	SSI Enable Register (SSIENR)	S/U
0x000C	Microwire Control Register (MWCR)	S/U
0x0010	Slave Select Register (SER)	S/U
0x0014	Baud Rate Select Register (BAUDR)	S/U
0x0018	Transmit FIFO Threshold Level Register (TXFTLR)	S/U
0x001C	Receive FIFO Threshold Level Register (RXFTLR)	S/U
0x0020	Transmit FIFO Level Register (TXFLR)	S/U
0x0024	Receive FIFO Level Register (RXFLR)	S/U
0x0028	Status Register (SR)	S/U
0x002C	Interrupt Mask Register (IMR)	S/U
0x0030	Interrupt Status Register (ISR)	S/U
0x0034	Raw Interrupt Status Register (RISR)	S/U
0x0038	Transmit FIFO Overflow Interrupt Clear Register (TXOICR)	S/U
0x003C	Receive FIFO Overflow Interrupt Clear Register (RXOICR)	S/U
0x0040	Receive FIFO Underflow Interrupt Clear Register (RXUICR)	S/U
0x0048	Interrupt Clear Register (ICR)	S/U
0x004C	DMA Control Register (DMACR)	S/U
0x0050	DMA Transmit Data Level Register (DMATDLR)	S/U
0x0054	DMA Receive Data Level Register (DMARDLR)	S/U
0x0058	Identification Register (IDR)	S/U
0x005C	Version ID Register (VIDR)	S/U
0x0060+i*0x4	SSI Data Register (DRx)	S/U
0x00F0	RX Sample Delay Register (RXSDR)	S/U
0x00F4	SPI Control Register 0 (SPICTRLR0)	S/U
0x00FC	XIP Mode Bits (XIPMBR)	S/U
0x0100	XIP Incr Inst Register (XIPIIR)	S/U
0x0104	XIP Wrap Inst Register (XIPWIR)	S/U
0x0108	XIP Control Register (XIPCR)	S/U
0x010C	XIP Slave Enable Register (XIPSER)	S/U
0x0110	XIP Receive FIFO Overflow Interrupt Clear Register (XRXIOCR)	S/U
0x0114	XIP Continus Transfer Time Out Register (XIPCTTOR)	S/U

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21.6.2. Register Descriptions

21.6.2.1. Control Register 0 (CTRLR0)

Address: QSPIn_BASEADDR+0x0000_0000

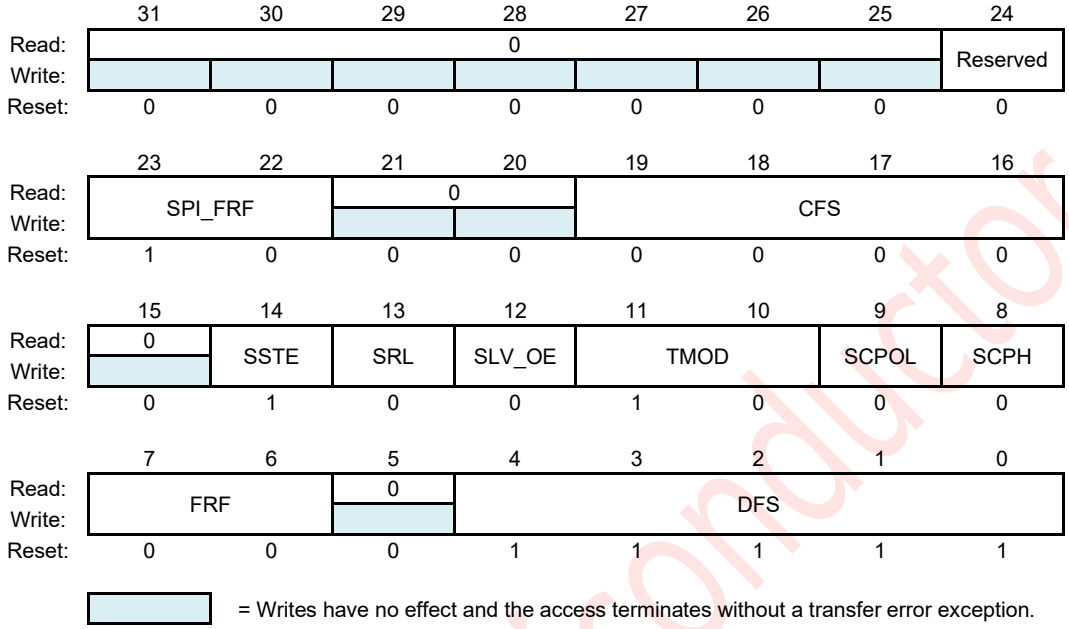


Figure 21-3: Control Register 0 (CTRLR0)

This register controls the serial data transfer. It is impossible to write to this register when the SSI is enabled. The SSI is enabled and disabled by writing to the SSIENR.

SPI_FRF — SPI Frame Format

Selects data frame format for Transmitting/Receiving the data bits only valid when SSIC_SPI_MODE is either set to "Dual" or "Quad" or "Octal" mode.

0x0 (SPI_STANDARD): Standard SPI Format
0x1 (SPI_DUAL): Dual SPI Format
0x2 (SPI_QUAD): Quad SPI Format
0x3 (SPI_OCTAL): Octal SPI Format

CFS — Control Frame Size

Selects the length of the control word for the Microwire frame format.

0x0 (SIZE_01_BIT): 1-bit Control Word
0x1 (SIZE_02_BIT): 2-bits Control Word
0x2 (SIZE_03_BIT): 3-bits Control Word
0x3 (SIZE_04_BIT): 4-bits Control Word
0x4 (SIZE_05_BIT): 5-bits Control Word
0x5 (SIZE_06_BIT): 6-bits Control Word
0x6 (SIZE_07_BIT): 7-bits Control Word
0x7 (SIZE_08_BIT): 8-bits Control Word
0x8 (SIZE_09_BIT): 9-bits Control Word
0x9 (SIZE_10_BIT): 10-bits Control Word

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0xA (SIZE_11_BIT): 11-bits Control Word
0xB (SIZE_12_BIT): 12-bits Control Word
0xC (SIZE_13_BIT): 13-bits Control Word
0xD (SIZE_14_BIT): 14-bits Control Word
0xE (SIZE_15_BIT): 15-bits Control Word
0xF (SIZE_16_BIT): 16-bits Control Word

SSTE — Slave Select Toggle Enable.

While operating in SPI mode with clock phase (SCPH) set to 0, this register controls the behavior of the slave select line (ss_*_n) between data frames.

1 = (TOGGLE_EN): ss_*_n line will toggle between consecutive data frames, with the serial clock (sclk) being held to its default value while ss_*_n is high
0 = (TOGGLE_DISABLE): ss_*_n will stay low and sclk will run continuously for the duration of the transfer

SRL — Shift Register Loop.

Used for testing purposes only. When internally active, connects the transmit shift register output to the receive shift register input. Can be used in both serial-slave and serial-master modes. When the SSI is configured as a slave in loopback mode, the ss_in_n and ssi_clk signals must be provided by an external source. In this mode, the slave cannot generate these signals because there is nothing to which to loop back.

1 = (TESTING_MODE): Test Mode Operation
0 = (NORMAL_MODE): Normal mode operation

SLV_OE — Slave Output Enable.

Relevant only when the SSI is configured as a serial-slave device. When configured as a serial master, this bit field has no functionality.

1 = Slave Output is disabled
0 = Slave Output is enabled

TMOD — Transfer Mode.

Selects the mode of transfer for serial communication. This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid.

0x0 (TX_AND_RX): Transmit & Receive; Not Applicable in enhanced SPI operating mode
0x1 (TX_ONLY): Transmit only mode; Or Write in enhanced SPI operating mode
0x2 (RX_ONLY): Receive only mode; Or Read in enhanced SPI operating mode
0x3 (EEPROM_READ): EEPROM Read mode; Not Applicable in enhanced SPI operating mode

SCPOL — Serial Clock Polarity.

Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the SSI master is not actively transferring data on the serial bus.

1 = (INACTIVE_HIGH): Inactive state of serial clock is high
0 = (INACTIVE_LOW): Inactive state of serial clock is low

SCPH — Serial Clock Phase.

Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal.

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When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock.

1 = (START_BIT): Serial clock toggles at start of first bit

0 = (MIDDLE_BIT): Serial clock toggles in middle of first bit

FRF — Frame Format.

Selects which serial protocol transfers the data.

0x0 (SPI): Motorola SPI Frame Format

0x1 (SSP): Texas Instruments SSP Frame Format

0x2 (MICROWIRE): National Semiconductors Microwire Frame Format

0x3 (RESERVED): Reserved

DFS — Data Frame Size.

Selects the data frame length. When the data frame size is programmed to be less than 32-bits, the receive data is automatically right-justified by the receive logic, with the upper bits of the receive FIFO zero-padded.

You must right-justify transmit data before writing into the transmit FIFO. The transmit logic ignores the upper unused bits when transmitting the data.

0x0 (DFS_01_BIT): Reserved

0x1 (DFS_02_BIT): Reserved

0x2 (DFS_03_BIT): Reserved

0x3 (DFS_04_BIT): 4-bits serial data transfer

0x4 (DFS_05_BIT): 5-bits serial data transfer

0x5 (DFS_06_BIT): 6-bits serial data transfer

0x6 (DFS_07_BIT): 7-bits serial data transfer

0x7 (DFS_08_BIT): 8-bits serial data transfer

0x8 (DFS_09_BIT): 9-bits serial data transfer

0x9 (DFS_10_BIT): 10-bits serial data transfer

0xA (DFS_11_BIT): 11-bits serial data transfer

0xB (DFS_12_BIT): 12-bits serial data transfer

0xC (DFS_13_BIT): 13-bits serial data transfer

0xD (DFS_14_BIT): 14-bits serial data transfer

0xE (DFS_15_BIT): 15-bits serial data transfer

0xF (DFS_16_BIT): 16-bits serial data transfer

0x10 (DFS_17_BIT): 17-bits serial data transfer

0x11 (DFS_18_BIT): 18-bits serial data transfer

0x12 (DFS_19_BIT): 19-bits serial data transfer

0x13 (DFS_20_BIT): 20-bits serial data transfer

0x14 (DFS_21_BIT): 21-bits serial data transfer

0x15 (DFS_22_BIT): 22-bits serial data transfer

0x16 (DFS_23_BIT): 23-bits serial data transfer

0x17 (DFS_24_BIT): 24-bits serial data transfer

0x18 (DFS_25_BIT): 25-bits serial data transfer

0x19 (DFS_26_BIT): 26-bits serial data transfer

0x1A (DFS_27_BIT): 27-bits serial data transfer

0x1B (DFS_28_BIT): 28-bits serial data transfer

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0x1C (DFS_29_BIT): 29-bits serial data transfer
0x1D (DFS_30_BIT): 30-bits serial data transfer
0x1E (DFS_31_BIT): 31-bits serial data transfer
0x1F (DFS_32_BIT): 32-bits serial data transfer

21.6.2.2. Control Register 1 (CTRLR1)

This register exists only when the SSI is configured as a master device. When the SSI is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. Control register 1 controls the end of serial transfers when in RX-ONLY mode and TX-ONLY mode. It is impossible to write to this register when the SSI is enabled. The SSI is enabled and disabled by writing to the SSIENR register.

Address: QSPIn_BASEADDR+0x0000_0004

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	NDF[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	NDF[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-4: Control Register 1 (CTRLR1)

NDF[15:0] — Number of Data Frames.

When TMOD = 01 or TMOD = 10 or TMOD = 11, this register field sets the number of data frames to be continuously received or transmitted by the SSI. The SSI continues to receive or transmit serial data until the number of data frames is equal to this register value plus 1. This register serves no purpose and is not present when the SSI is configured as a serial slave. When TMOD = 01, CLK_STRETCH_EN in SPI_CTRLR0 must be set.

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21.6.2.3. SSI Enable Register (SSIENR)

Address: QSPIn_BASEADDR+0x0000_0008

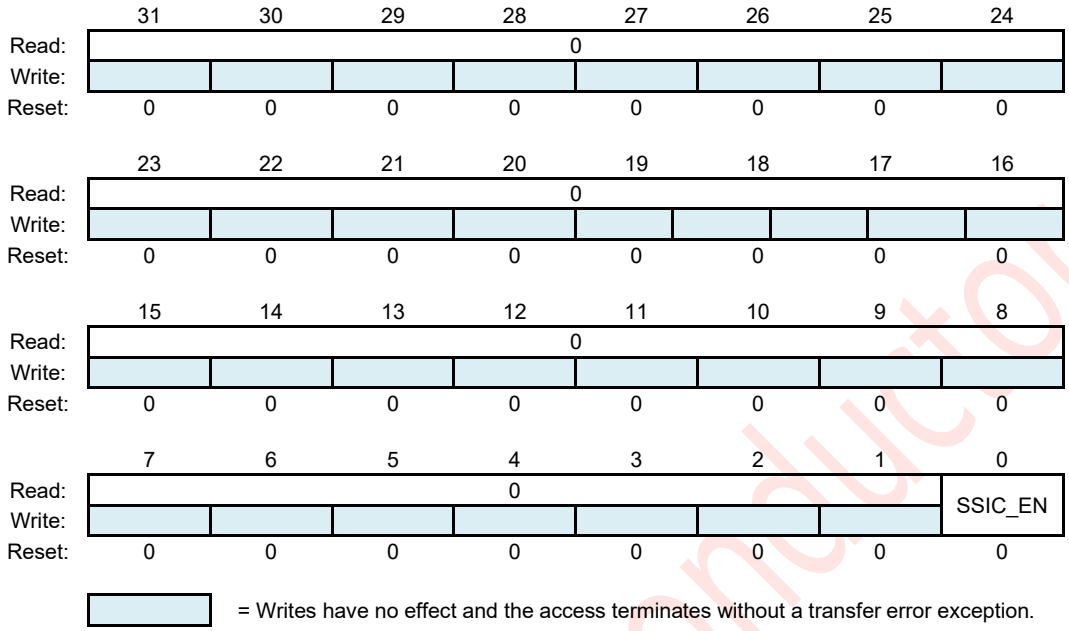


Figure 21-5: SSI Enable Register (SSIENR)

SSIC_EN — SSI Enable.

Enables and disables all SSI operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the SSI control registers when enabled. When disabled, the SSI sleep output is set (after delay) to inform the system that it is safe to remove the ssi_clk, thus saving power consumption in the system.

1 = SSI is enabled.

0 = SSI is disabled.

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21.6.2.4. Microwire Control Register (MWCR)

Address: QSPIn_BASEADDR+0x0000_000C

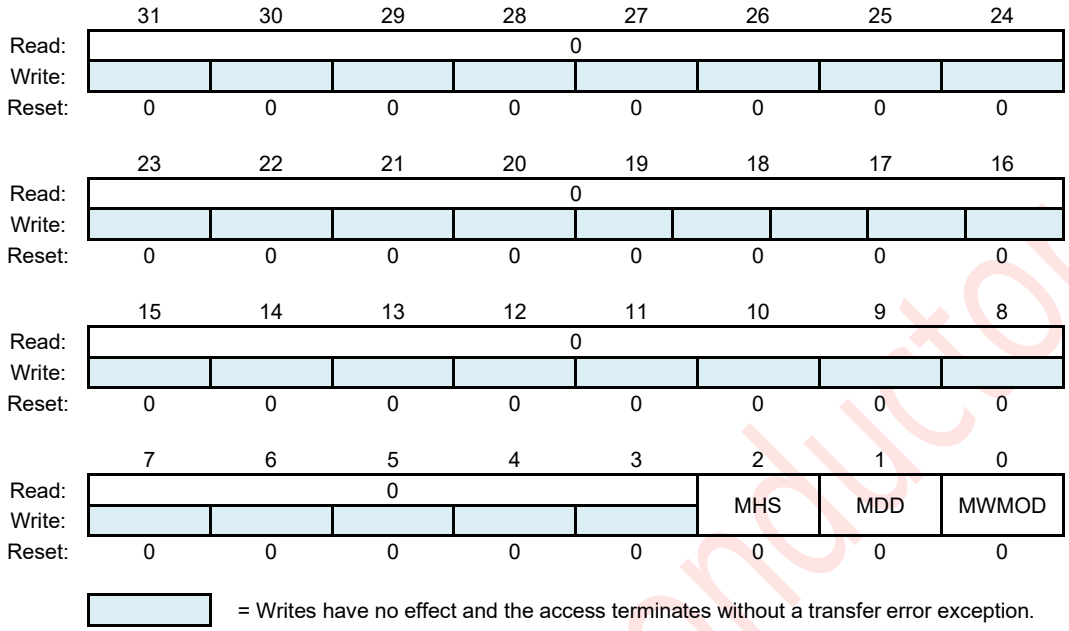


Figure 21-6: Microwire Control Register (MWCR)

This register controls the direction of the data word for the half-duplex Microwire serial protocol. It is impossible to write to this register when the SSI is enabled. The SSI is enabled and disabled by writing to the SSIENR register.

MHS — Microwire Handshaking.

Relevant only when the SSI is configured as a serial-master device. When configured as a serial slave, this bit field has no functionality. Used to enable and disable the busy/ready handshaking interface for the Microwire protocol. When enabled, the SSI checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register.

1 = handshaking interface is enabled

0 = handshaking interface is disabled

MDD — Microwire Control.

Defines the direction of the data word when the Microwire serial protocol is used. When this bit is set to 0, the data word is received by the SSI MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the SSI MacroCell to the external serial device.

1 = SSI transmits data

0 = SSI receives data

MWMOD — Microwire Transfer Mode.

Defines whether the Microwire transfer is sequential or non-sequential. When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received.

1 = Sequential Transfer

0 = Non-Sequential Transfer

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21.6.2.5. Slave Enable Register (SER)

Address: QSPIn_BASEADDR+0x0000_0010

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0							SER
Write:								
Reset:	0	0	0	0	0	0	0	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-7: Slave Enable Register (SER)

This register is valid only when the SSI is configured as a master device. When the SSI is configured as a serial slave, writing to this location has no effect; reading from this location returns 0. The register enables the individual slave select output lines from the SSI master. Up to 16 slave-select output pins are available on the SSI master. You cannot write to this register when SSI is busy and when SSIC_EN = 1.

SER — Slave Select Enable Flag.

1 = Selected

0 = Not Selected

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21.6.2.6. Baud Rate Select (BAUDR)

Address: QSPIn_BASEADDR+0x0000_0014

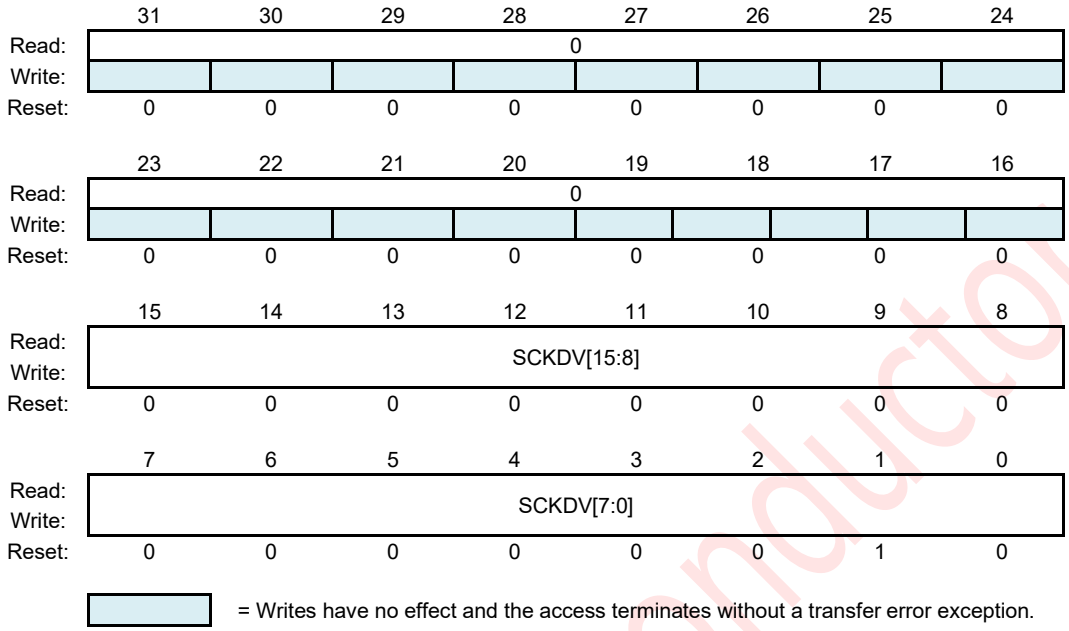


Figure 21-8: Baud Rate Select (BAUDR)

SCKDV[15:0] — SSI Clock Divider.

The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation:

Fsclk_out = Fssi_clk / SCKDV

Where SCKDV is any even value between 2 and 65534. For example: for Fssi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2 = 1.8432MHz.

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21.6.2.7. Transmit FIFO Threshold Level (TXFTLR)

Address: QSPIn_BASEADDR+0x0000_0018

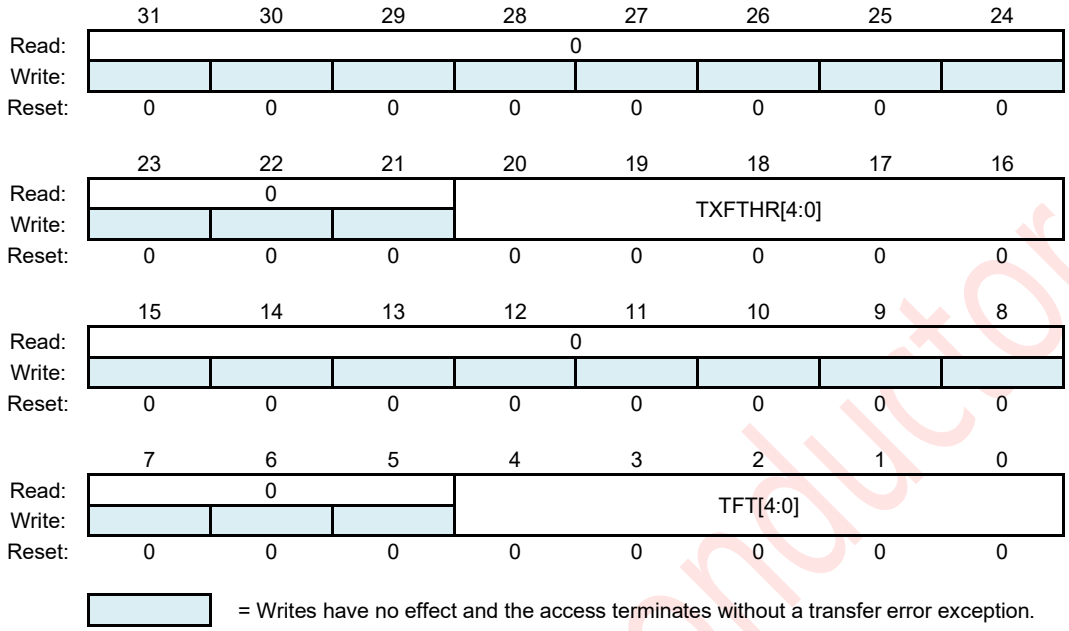


Figure 21-9: Transmit FIFO Threshold Level (TXFTLR)

This register controls the threshold value for the transmit FIFO memory. The SSI is enabled and disabled by writing to the SSIENR register.

TXFTHR[4:0] — Transfer start FIFO level.

Used to control the level of entries in transmit FIFO above which transfer will start on serial line. This register can be used to ensure that sufficient data is present in transmit FIFO before starting a write operation on serial line. These field is valid only for Master mode of operation.

TFT[4:0] — Transmit FIFO Threshold.

Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 8-256; this register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

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21.6.2.8. Receive FIFO Threshold Level (RXFTLR)

Address: QSPIn_BASEADDR+0x0000_001C

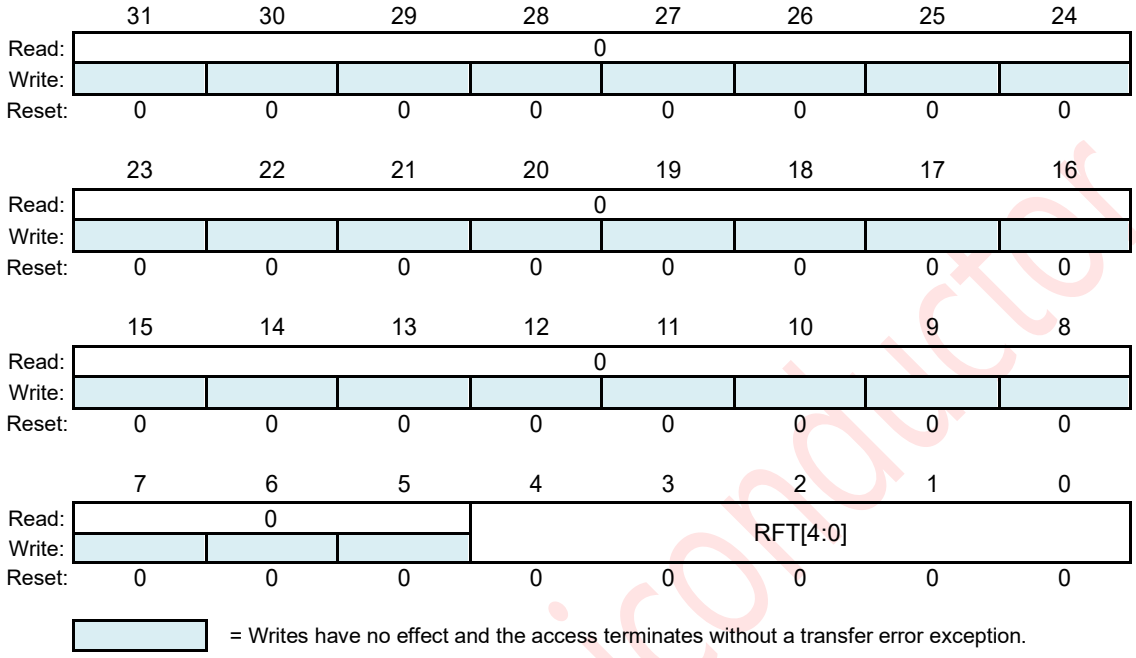


Figure 21-10: Receive FIFO Threshold Level (RXFTLR)

This register controls the threshold value for the receive FIFO memory. The SSI is enabled and disabled by writing to the SSIENR register.

RFT[4:0] — Receive FIFO Threshold.

Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. This register is sized to the number of address bits needed to access the FIFO. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

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21.6.2.9. Transmit FIFO Level Register (TXFLR)

Address: QSPIn_BASEADDR+0x0000_0020

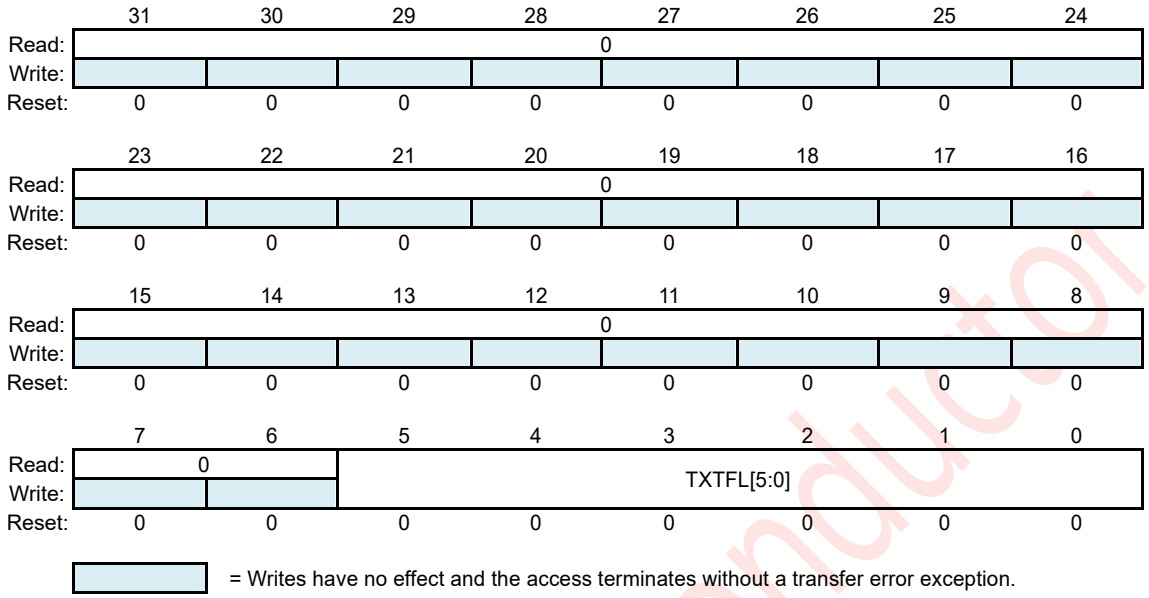


Figure 21-11: Transmit FIFO Level Register (TXFLR)

TXTFL[5:0] — Transmit FIFO Level.

Contains the number of valid data entries in the transmit FIFO.

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21.6.2.10. Receive FIFO Level Register (RXFLR)

Address: QSPIn_BASEADDR+0x0000_0024

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0		RXTFL[5:0]					
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-12: Receive FIFO Level Register (RXFLR)

RXTFL[5:0] — Receive FIFO Level.

Contains the number of valid data entries in the receive FIFO.

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21.6.2.11. Status Register (SR)

Address: QSPIn_BASEADDR+0x0000_0028

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0	Reserved	TXE	RFF	RFNE	TFE	TFNF	BUSY
Write:								
Reset:	0	0	0	0	0	1	1	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-13: Status Register (SR)

TXE — Transmission Error.

Set if the transmit FIFO is empty when a transfer is started. This bit can be set only when the SSI is configured as a slave device. Data from the previous transmission is resent on the TXD line. This bit is cleared when read.

1 = (TX_ERROR): Transmission Error

0 = (NO_ERROR): No Error

RFF — Receive FIFO Full.

When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared.

1 = (FULL): Receive FIFO is full

0 = (NOT_FULL): Receive FIFO is not full

RFNE — Receive FIFO Not Empty.

Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO.

1 = (NOT_EMPTY): Receive FIFO is not empty

0 = (EMPTY): Receive FIFO is empty

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TFE — Transmit FIFO Empty.

When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt.

1 = (EMPTY): Transmit FIFO is empty

0 = (NOT_EMPTY): Transmit FIFO is not empty

TFNF — Transmit FIFO Not Full.

Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.

1 = (NOT_FULL): Tx FIFO is not Full

0 = Tx FIFO is full

BUSY — SSI Busy Flag.

When set, indicates that a serial transfer is in progress; when cleared indicates that the SSI is idle or disabled.

1 = (ACTIVE): SSI is actively transferring data

0 = (INACTIVE): SSI is idle or disabled

21.6.2.12. Interrupt Mask Register (IMR)

Address: QSPIn_BASEADDR+0x0000_002C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0	XRXOIM	Reserved	RXFIM	RXOIM	RXUIM	TXOIM	TXEIM
Write:								
Reset:	0	1	1	1	1	1	1	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-14: Interrupt Mask Register (IMR)

XRXOIM — XIP Receive FIFO Overflow Interrupt Mask

1 = (UNMASKED): ssi_xrxo_intr interrupt is not masked

0 = (MASKED): ssi_xrxo_intr interrupt is masked

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RXFIM — Receive FIFO Full Interrupt Mask

1 = (UNMASKED): ssi_rxf_intr interrupt is not masked
0 = (MASKED): ssi_rxf_intr interrupt is masked

RXOIM — Receive FIFO Overflow Interrupt Mask

1 = (UNMASKED): ssi_rxo_intr interrupt is not masked
0 = (MASKED): ssi_rxo_intr interrupt is masked

RXUIM — Receive FIFO Underflow Interrupt Mask

1 = (UNMASKED): ssi_rxu_intr interrupt is not masked
0 = (MASKED): ssi_rxu_intr interrupt is masked

TXOIM — Transmit FIFO Overflow Interrupt Mask

1 = (UNMASKED): ssi_txo_intr interrupt is not masked
0 = (MASKED): ssi_txo_intr interrupt is masked

TXEIM — Transmit FIFO Empty Interrupt Mask

1 = (UNMASKED): ssi_txe_intr interrupt is not masked
0 = (MASKED): ssi_txe_intr interrupt is masked

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21.6.2.13. Interrupt Status Register (ISR)

Address: QSPIn_BASEADDR+0x0000_0030

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0	XRXOIS	Reserved	RXFIS	RXOIS	RXUIS	TXOIS	TXEIS
Write:								
Reset:	0	0	0	0	0	0	0	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-15: Interrupt Status Register (ISR)

This register reports the status of the SSI interrupts after they have been masked.

XRXOIS — XIP Receive FIFO Overflow Interrupt Status

1 = (ACTIVE): ssi_xrxo_intr interrupt is active after masking

0 = (INACTIVE): ssi_xrxo_intr interrupt is not active after masking

RXFIS — Receive FIFO Full Interrupt Status

1 = (ACTIVE): ssi_rxf_intr interrupt is active after masking

0 = (INACTIVE): ssi_rxf_intr interrupt is not active after masking

RXOIS — Receive FIFO Overflow Interrupt Status

1 = (ACTIVE): ssi_rxo_intr interrupt is active after masking

0 = (INACTIVE): ssi_rxo_intr interrupt is not active after masking

RXUIS — Receive FIFO Underflow Interrupt Status

1 = (ACTIVE): ssi_rxu_intr interrupt is active after masking

0 = (INACTIVE): ssi_rxu_intr interrupt is not active after masking

TXOIS — Transmit FIFO Overflow Interrupt Status

1 = (ACTIVE): ssi_txo_intr interrupt is active after masking

0 = (INACTIVE): ssi_txo_intr interrupt is not active after masking

TXEIS — Transmit FIFO Empty Interrupt Status

1 = (ACTIVE): ssi_txe_intr interrupt is active after masking

0 = (INACTIVE): ssi_txe_intr interrupt is not active after masking

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21.6.2.14. Raw Interrupt Status Register (RISR)

Address: QSPIn_BASEADDR+0x0000_0034

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0	XRXOIS	Reserved	RXFIS	RXOIS	RXUIS	TXOIS	TXEIS
Write:								
Reset:	0	0	0	0	0	0	0	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-16: Raw Interrupt Status Register (RISR)

XRXOIS — XIP Receive FIFO Overflow Raw Interrupt Status

1 = (ACTIVE): ssi_xrxo_intr interrupt is active prior to masking

0 = (INACTIVE): ssi_xrxo_intr interrupt is not active prior masking

RXFIS — Receive FIFO Full Raw Interrupt Status

1 = (ACTIVE): ssi_rxf_intr interrupt is active prior to masking

0 = (INACTIVE): ssi_rxf_intr interrupt is not active prior masking

RXOIS — Receive FIFO Overflow Raw Interrupt Status

1 = (ACTIVE): ssi_rxo_intr interrupt is active prior to masking

0 = (INACTIVE): ssi_rxo_intr interrupt is not active prior masking

RXUIS — Receive FIFO Underflow Raw Interrupt Status

1 = (ACTIVE): ssi_rxu_intr interrupt is active prior to masking

0 = (INACTIVE): ssi_rxu_intr interrupt is not active prior masking

TXOIS — Transmit FIFO Overflow Raw Interrupt Status

1 = (ACTIVE): ssi_txo_intr interrupt is active prior to masking

0 = (INACTIVE): ssi_txo_intr interrupt is not active prior masking

TXEIS — Transmit FIFO Empty Raw Interrupt Status

1 = (ACTIVE): ssi_txe_intr interrupt is active prior to masking

0 = (INACTIVE): ssi_txe_intr interrupt is not active prior masking

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21.6.2.15. Transmit FIFO Overflow Interrupt Clear Registers (TXOICR)

Address: QSPIn_BASEADDR+0x0000_0038

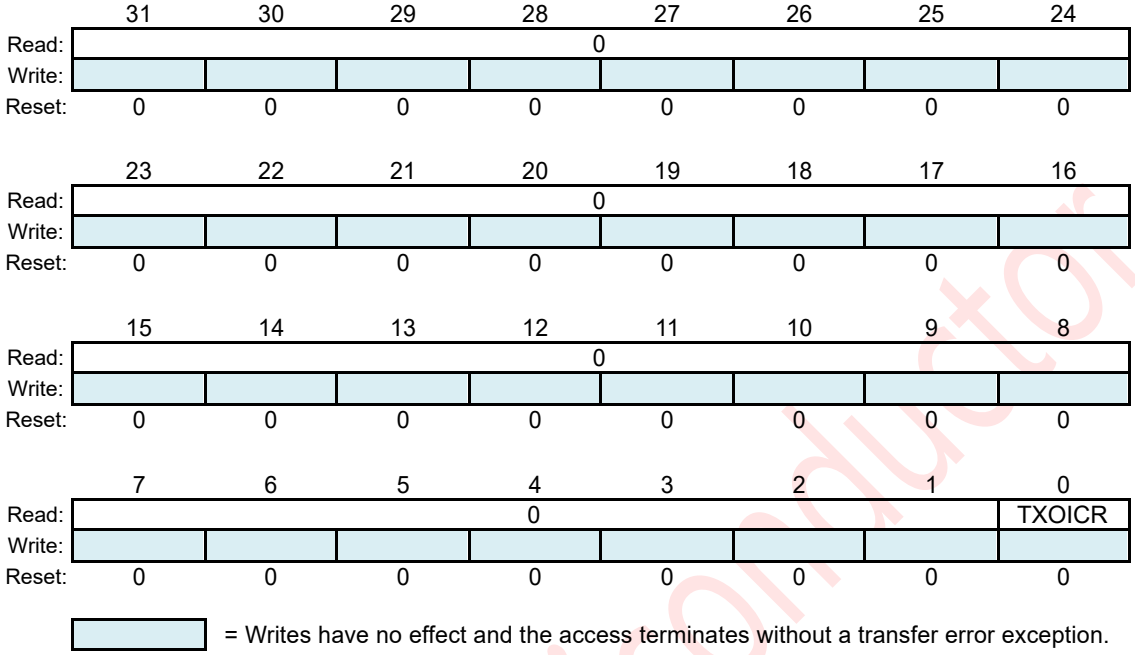


Figure 21-17: Transmit FIFO Overflow Interrupt Clear Registers (TXOICR)

TXOICR — Clear Transmit FIFO Overflow Interrupt.

This register reflects the status of the interrupt. A read from this register clears the ssi_txo_intr interrupt; writing has no effect.

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21.6.2.16. Receive FIFO Overflow Interrupt Clear Register (RXOICR)

Address: QSPIn_BASEADDR+0x0000_003C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0							RXOICR
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-18: Receive FIFO Overflow Interrupt Clear Register (RXOICR)

RXOICR — Clear Receive FIFO Overflow Interrupt.

This register reflects the status of the interrupt. A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.

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21.6.2.17. Receive FIFO Underflow Interrupt Clear Register (RXUICR)

Address: QSPIn_BASEADDR+0x0000_0040

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0							RXUICR
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-19: Receive FIFO Underflow Interrupt Clear Register (RXUICR)

RXUICR — Clear Receive FIFO Underflow Interrupt.

This register reflects the status of the interrupt. A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.

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21.6.2.18. Interrupt Clear Register (ICR)

Address: QSPIn_BASEADDR+0x0000_0048

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0							ICR
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-20: Interrupt Clear Register (ICR)

ICR — Clear Interrupts.

This register is set if any of the interrupts below are active. A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

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21.6.2.19. DMA Control Register (DMACR)

Address: QSPIn_BASEADDR+0x0000_004C

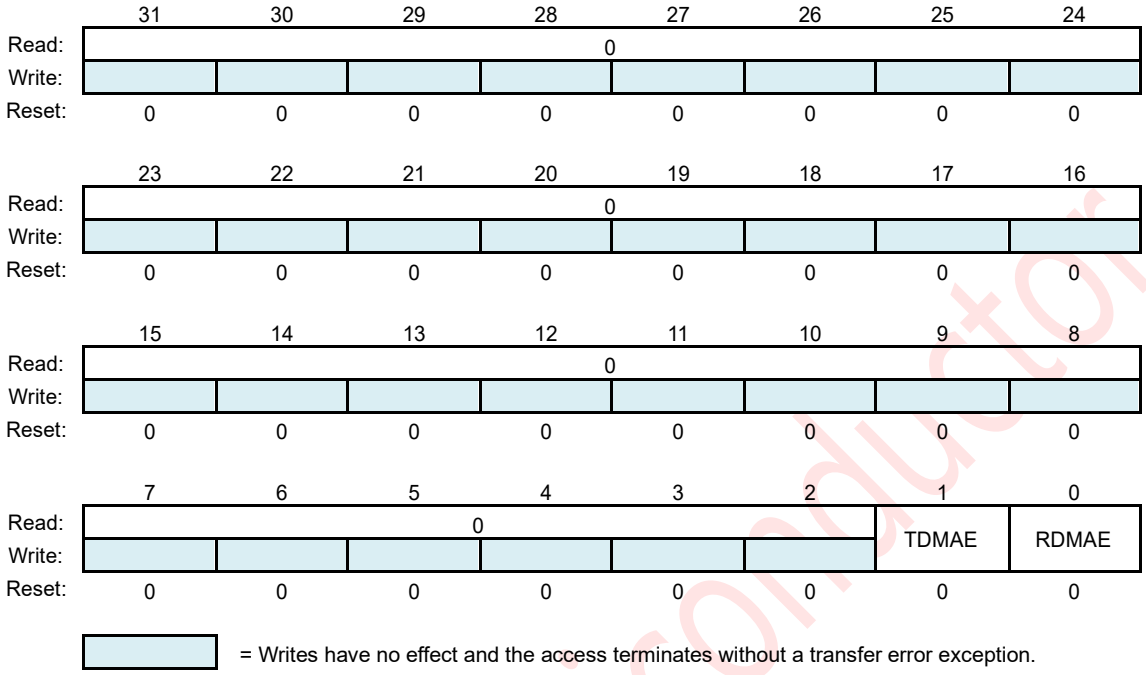


Figure 21-21: DMA Control Register (DMACR)

This register is only valid when SSI is configured with a set of DMA Controller interface signals (SSIC_HAS_DMA = 1). When SSI is not configured for DMA operation, this register will not exist and writing to the register's address will have no effect; reading from this register address will return zero. The register is used to enable the DMA Controller interface operation.

TDMAE — Transmit DMA Enable

This bit enables/disables the transmit FIFO DMA channel.

1 = Transmit DMA is enabled

0 = Transmit DMA is disabled

RDMAE — Receive DMA Enable

This bit enables/disables the receive FIFO DMA channel.

1 = Receive DMA is enabled

0 = Receive DMA is disabled

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21.6.2.20. DMA Transmit Data Level (DMATDLR)

Address: QSPIn_BASEADDR+0x0000_0050

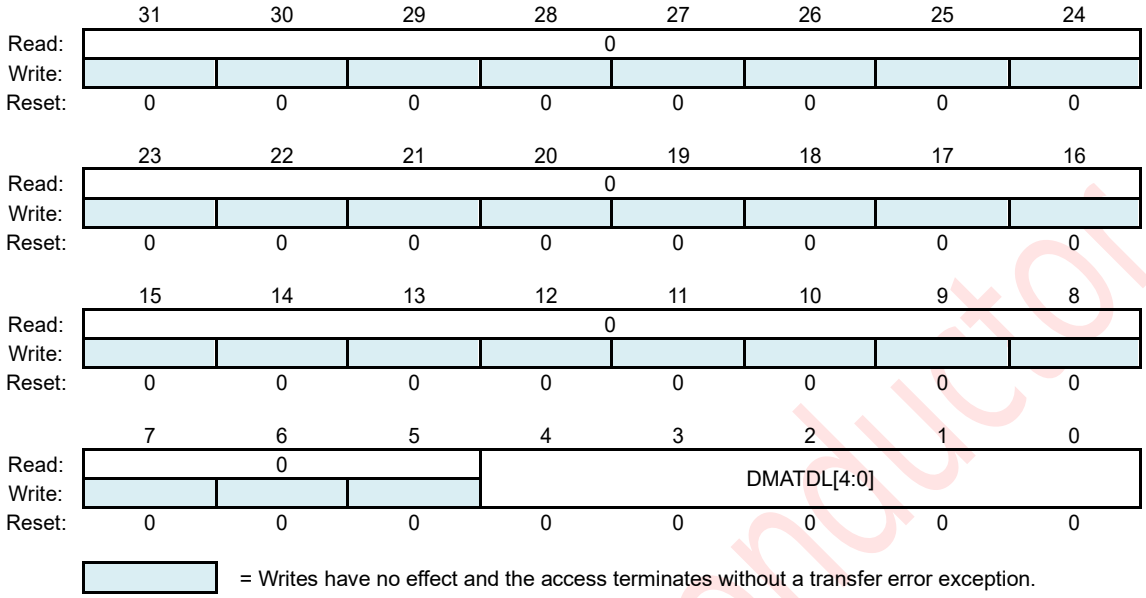


Figure 21-22: DMA Transmit Data Level (DMATDLR)

This register is only valid when the SSI is configured with a set of DMA interface signals (SSIC_HAS_DMA = 1). When SSI is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero.

DMATDL[4:0] — Transmit Data Level.

This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

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21.6.2.21. DMA Receive Data Level (DMARDLR)

Address: QSPIn_BASEADDR+0x0000_0054

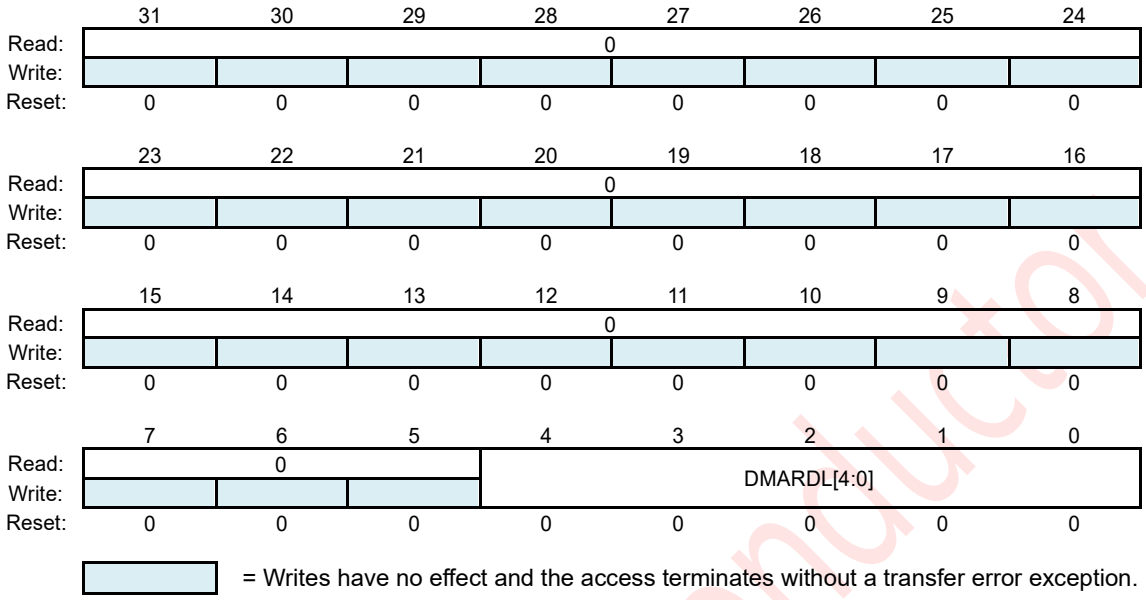


Figure 21-23: DMA Receive Data Level (DMARDLR)

This register is only valid when SSI is configured with a set of DMA interface signals (SSIC_HAS_DMA = 1). When SSI is not configured for DMA operation, this register will not exist and writing to its address will have no effect; reading from its address will return zero.

DMARDL[4:0] — Receive Data Level.

This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE = 1.

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21.6.2.22. Identification Register (IDR)

Address: QSPIn_BASEADDR+0x0000_0058

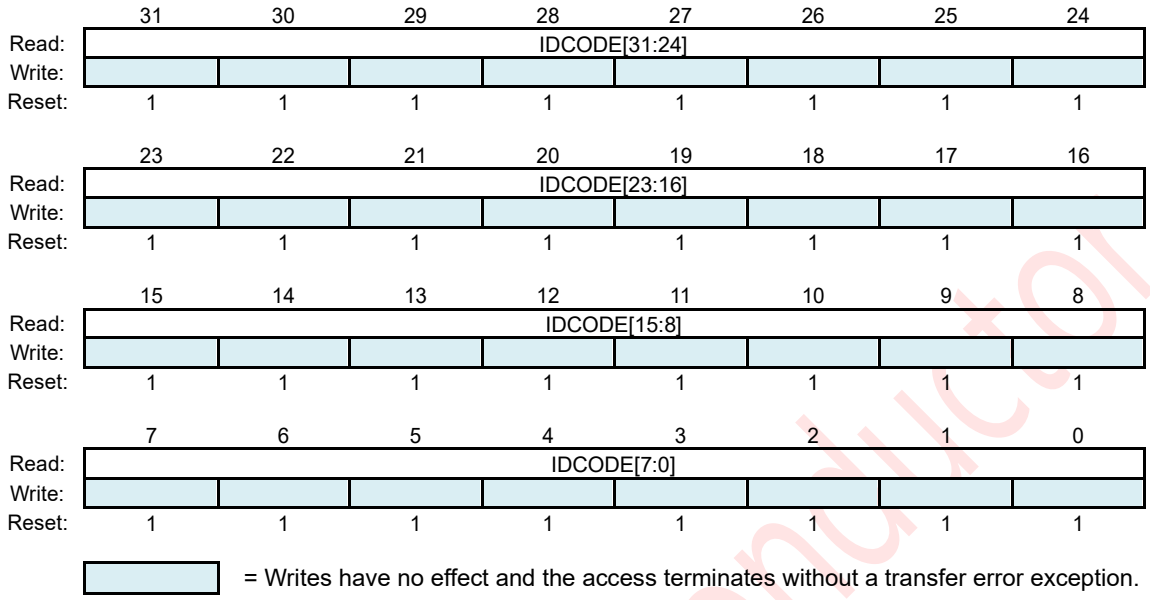


Figure 21-24: Identification Register (IDR)

IDCODE[31:0] — Identification code.

The register contains the peripheral's identification code, which is written into the register at configuration time using CoreConsultant.

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21.6.2.23. Version ID Register (VIDR)

Address: QSPIn_BASEADDR+0x0000_005C

	31	30	29	28	27	26	25	24
Read:	SSIC_COMP_VERSION[31:24]							
Write:								
Reset:	0	0	1	1	0	0	0	1

	23	22	21	20	19	18	17	16
Read:	SSIC_COMP_VERSION[23:16]							
Write:								
Reset:	0	0	1	1	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	SSIC_COMP_VERSION[15:8]							
Write:								
Reset:	0	0	1	1	0	0	0	1

	7	6	5	4	3	2	1	0
Read:	SSIC_COMP_VERSION[7:0]							
Write:								
Reset:	0	0	1	0	1	0	1	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-25: Version ID Register (VIDR)

SSIC_COMP_VERSION[31:0]

Contains the hex representation of the Synopsys component version. Consists of ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01*.

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21.6.2.24. SSI Data Register (DRx)

Address: QSPIn_BASEADDR+0x0000_0060

	31	30	29	28	27	26	25	24
Read: Write:	DR[31:24]							
Reset:	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
Read: Write:	DR[23:16]							
Reset:	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
Read: Write:	DR[15:8]							
Reset:	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
Read: Write:	DR[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 21-26: SSI Data Register (DRx)

The SSI data register is a 32-bits read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSIC_EN = 1. FIFOs are reset when SSIC_EN = 0.

DR[31:0] — Data Register.

When writing to this register, you must right-justify the data. Read data are automatically right-justified.

Read = Receive FIFO buffer

Write = Transmit FIFO buffer.

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21.6.2.25. RX Sample Delay Register (RXSDR)

Address: QSPIn_BASEADDR+0x0000_00F0

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							SE
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	RSD[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-27: RX Sample Delay Register (RXSDR)

SE — Receive Data (RXD) Sampling Edge.

1 = negative edge of ssi_clk will be used to sample the incoming data

0 = postive edge of ssi_clk will be used to sample the incoming data

RSD[7:0] — Receive Data (RXD) Sample Delay.

This register is used to delay the sample of the RXD input port. Each value represents a single ssi_clk delay on the sample of RXD.

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21.6.2.26. SPI Control Register 0 (SPICTRLR0)

Address: QSPIn_BASEADDR+0x0000_00F4

	31	30	29	28	27	26	25	24
Read:	0	CLK_STRETCH_EN	Reserved	0	Reserved			
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0	0	Reserved					
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	WAIT_CYCLES[4:0]					0	INST_L[1:0]	
Write:								
Reset:	0	0	0	0	0	0	1	0

	7	6	5	4	3	2	1	0
Read:	Reserved	0	ADDR_L[3:0]				TRANS_TYPE[1:0]	
Write:								
Reset:	0	0	0	1	1	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-28: SPI Control Register 0 (SPICTRLR0)

CLK_STRETCH_EN

Enables clock stretching capability in SPI transfers.

In case of write, if the FIFO becomes empty SSI will stretch the clock until FIFO has enough data to continue the transfer. In case of read, if the receive FIFO becomes full SSI will stop the clock until data has been read from the FIFO.

Note: recommend always to set this bit

1 = CLK_STRETCH_ENABLE

0 = CLK_STRETCH_DISABLE

WAIT_CYCLES[4:0] — Wait cycles in Dual/Quad/Octal mode between control frames transmit and data reception. Specified as number of SPI clock cycles.

INST_L[1:0] — Dual/Quad/Octal mode instruction length in bits.

0x0 (INST_L0): No Instruction

0x1 (INST_L4): 4-bits Instruction length

0x2 (INST_L8): 8-bits Instruction length

0x3 (INST_L16): 16-bits Instruction length

ADDR_L[3:0] — Length of Address to be transmitted

0x0 (ADDR_L0): No Address

0x1 (ADDR_L4): 4-bits Address length

0x2 (ADDR_L8): 8-bits Address length

0x3 (ADDR_L12): 12-bits Address length

0x4 (ADDR_L16): 16-bits Address length

0x5 (ADDR_L20): 20-bits Address length

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0x6 (ADDR_L24): 24-bits Address length
0x7 (ADDR_L28): 28-bits Address length
0x8 (ADDR_L32): 32-bits Address length
0x9 (ADDR_L36): 36-bits Address length
0xA (ADDR_L40): 40-bits Address length
0xB (ADDR_L44): 44-bits Address length
0xC (ADDR_L48): 48-bits Address length
0xD (ADDR_L52): 52-bits Address length
0xE (ADDR_L56): 56-bits Address length
0xF (ADDR_L60): 60-bits Address length

TRANS_TYPE[1:0] — Address and instruction transfer format.

Selects whether SSI will transmit instruction/address either in Standard SPI mode or the SPI mode selected in CTRLR0.SPI_FRF field.

0x0 (TT0): Instruction and Address will be sent in Standard SPI Mode.
0x1 (TT1): Instruction will be sent in Standard SPI Mode and Address will be sent in the mode specified by CTRLR0.SPI_FRF.
0x2 (TT2): Both Instruction and Address will be sent in the mode specified by SPI_FRF.
0x3 (TT3): Reserved.

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21.6.2.27. XIP Mode Bits (XIPMBR)

Address: QSPIn_BASEADDR+0x0000_00FC

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	XIP_MD_BITS[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	XIP_MD_BITS]7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-29: XIP Mode Bits (XIPMBR)

This register carries the mode bits which are sent in the XIP mode of operation after address phase. This is an 8-bits register and can only be written when SSIENR register is set to 0.

XIP_MD_BITS[15:0]

XIP mode bits to be sent after address phase of XIP transfer.

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21.6.2.28. XIP Incr Inst Register (XIPIIR)

Address: QSPIn_BASEADDR+0x0000_0100

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	INCR_INST[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	INCR_INST[7:0]							
Write:								
Reset:	0	1	1	0	1	0	1	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-30: **XIP Incr Inst Register (XIPIIR)**

This Register is valid only when SSIC_XIP_INST_EN is equal to 1. This register is used to store the instruction op-code to be used in INCR transactions when the same is requested on AHB interface. It is not possible to write to this register when the SSI is enabled (SSIC_EN = 1). The SSI is enabled and disabled by writing to the SSIENR register.

INCR_INST[15:0] — XIP INCR transfer opcode.

When SPI_CTRLR0.XIP_INST_EN bit is set to 1, SSI sends instruction for all XIP transfers, this register field stores the instruction op-code to be sent when an INCR type transfer is requested on AHB bus. The number of bits to be send in instruction phase is determined by SPI_CTRL0.INST_L field.

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21.6.2.29. XIP Wrap Inst Register (XIPWIR)

Address: QSPIn_BASEADDR+0x0000_0104

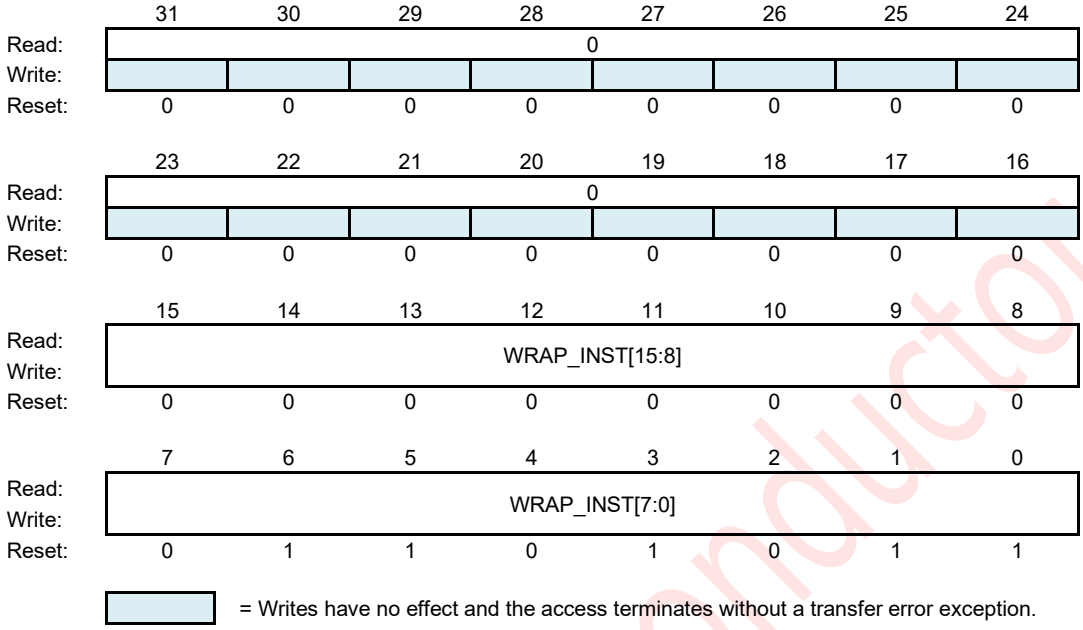


Figure 21-31: **XIP Wrap Inst Register (XIPWIR)**

This Register is valid only when SSIC_XIP_INST_EN is equal to 1. This register is used to store the instruction op-code to be used in WRAP transactions when the same is requested on AHB interface. It is not possible to write to this register when the SSI is enabled (SSIC_EN = 1). The SSI is enabled and disabled by writing to the SSIENR register.

WRAP_INST[15:0] — XIP WRAP transfer opcode.

When SPI_CTRLR0.XIP_INST_EN bit is set to 1, SSI sends instruction for all XIP transfers, this register field stores the instruction op-code to be sent when an WRAP type transfer is requested on AHB bus. The number of bits to be send in instruction phase is determined by SPI_CTRL0.INST_L field.

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21.6.2.30. XIP Control Register (XIPCR)

Address: QSPIn_BASEADDR+0x0000_0108

	31	30	29	28	27	26	25	24
Read:	0	0	XIP_PREFETCH_EN	0	XIP_MBL[1:0]		Reserved	
Write:								
Reset:	0	0	1	0	1	0	0	0

	23	22	21	20	19	18	17	16
Read:	CONT_XFER_EN	INST_EN	Reserved				WAIT_CYCLES[4:3]	
Write:								
Reset:	1	1	0	0	0	0	0	1

	15	14	13	12	11	10	9	8
Read:	WAIT_CYCLES[2:0]			MD_BITS_EN	0	INST_L[1:0]		0
Write:								
Reset:	0	0	0	0	0	1	0	0

	7	6	5	4	3	2	1	0
Read:	ADDR_L[3:0]				TRANS_TYPE		FRF	
Write:								
Reset:	0	1	1	0	0	0	1	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-32: **XIP Control Register (XIPCR)**

This Register is valid only when SSIC_CONCURRENT_XIP_EN is equal to 1. This register is used to store the control information that the XIP transfer will be using in the concurrent mode.

XIP_PREFETCH_EN

1 = Enables XIP pre-fetch functionality in SSI.

0 = Disables XIP pre-fetch functionality in SSI.

XIP_MBL[1:0] — XIP Mode bits length.

Sets the length of mode bits in XIP mode of operation. These bits are valid only when XIP_CTRL.XIP_MD_BIT_EN is set to 1.

0x0 (MBL_2): Mode bits length equal to 2

0x1 (MBL_4): Mode bits length equal to 4

0x2 (MBL_8): Mode bits length equal to 8

0x3 (MBL_16): Mode bits length equal to 16

CONT_XFER_EN

1 = Enable continuous transfer in XIP mode.

0 = Disables continuous transfer in XIP mode.

INST_EN

1 = XIP transfers will have instruction phase.

0 = XIP transfers will not have instruction phase.

WAIT_CYCLES[4:0] — Wait cycles in Dual/Quad/Octal mode between control frames transmit and data reception. Specified as number of SPI clock cycles.

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MD_BITS_EN — Mode bits enable in XIP mode.

1 = insert mode bits after the address phase.

0 = no mode bits after the address phase.

INST_L[1:0]

Dual/Quad/Octal mode instruction length in bits.

0x0 (INST_L0): No Instruction

0x1 (INST_L4): 4-bits Instruction length

0x2 (INST_L8): 8-bits Instruction length

0x3 (INST_L16): 16-bits Instruction length

ADDR_L[3:0]

This bit defines Length of Address to be transmitted. Only after this much bits are programmed in to the FIFO the transfer can begin.

0x0 (ADDR_L0): No Address

0x1 (ADDR_L4): 4-bits Address length

0x2 (ADDR_L8): 8-bits Address length

0x3 (ADDR_L12): 12-bits Address length

0x4 (ADDR_L16): 16-bits Address length

0x5 (ADDR_L20): 20-bits Address length

0x6 (ADDR_L24): 24-bits Address length

0x7 (ADDR_L28): 28-bits Address length

0x8 (ADDR_L32): 32-bits Address length

0x9 (ADDR_L36): 36-bits Address length

0xA (ADDR_L40): 40-bits Address length

0xB (ADDR_L44): 44-bits Address length

0xC (ADDR_L48): 48-bits Address length

0xD (ADDR_L52): 52-bits Address length

0xE (ADDR_L56): 56-bits Address length

0xF (ADDR_L60): 60-bits Address length

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TRANS_TYPE[1:0]

Address and instruction transfer format.

Selects whether SSI will transmit instruction/address either in Standard SPI mode or the SPI mode selected in CTRLR0.SPI_FRF field.

0x0 (TT0): Instruction and Address will be sent in Standard SPI Mode.

0x1 (TT1): Instruction will be sent in Standard SPI Mode and Address will be sent in the mode specified by XIP_CTRL.SPI_FRF.

0x2 (TT2): Both Instruction and Address will be sent in the mode specified by XIP_CTRL.FRF.

0x3 (TT3): Reserved.

FRF[1:0] — SPI Frame Format

Selects data frame format for Transmitting/Receiving the data.

0x0 (RSVD): Reserved

0x1 (SPI_DUAL): Dual SPI Format

0x2 (SPI_QUAD): Quad SPI Format

0x3 (SPI_OCTAL): Octal SPI Format

21.6.2.31. XIP Slave Enable Register (XIPSER)

Address: QSPIn_BASEADDR+0x0000_010C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0							SER
Write:								
Reset:	0	0	0	0	0	0	0	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-33: XIP Slave Enable Register (XIPSER)

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This register is valid only when the SSIC_CONCURRENT_XIP_EN is equal to 1. The register enables the individual slave select output lines from the SSI master for XIP mode of operation. Up to 16 slave-select output pins are available on the SSI master. You cannot write to this register when SSI is busy or when SSIC_EN = 1.

SER — Slave Select Enable Flag.

Each bit in this register corresponds to a slave select line (ss_x_n) from the SSI master. When a bit in this register is set (1), the corresponding slave select line from the master is activated when a XIP transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a XIP transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

1 = Select

0 = Not Select

XIP Receive FIFO Overflow Interrupt Clear Register (XRXIOCR)

21.6.2.32. XIP Receive FIFO Overflow Interrupt Clear Register (XRXIOCR)

Address: QSPIn_BASEADDR+0x0000_0110

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0							XRXOICR
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 21-34: XIP Receive FIFO Overflow Interrupt Clear Register (XRXIOCR)

XRXOICR — Clear XIP Receive FIFO Overflow Interrupt.

This register reflects the status of the interrupt. A read from this register clears the ssi_xrxo_intr(_n) interrupt; writing has no effect.

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21.6.2.33. XIP Continus Transfer Time Out Register (XIPCTTOR)

Address: QSPIn_BASEADDR+0x0000_0114

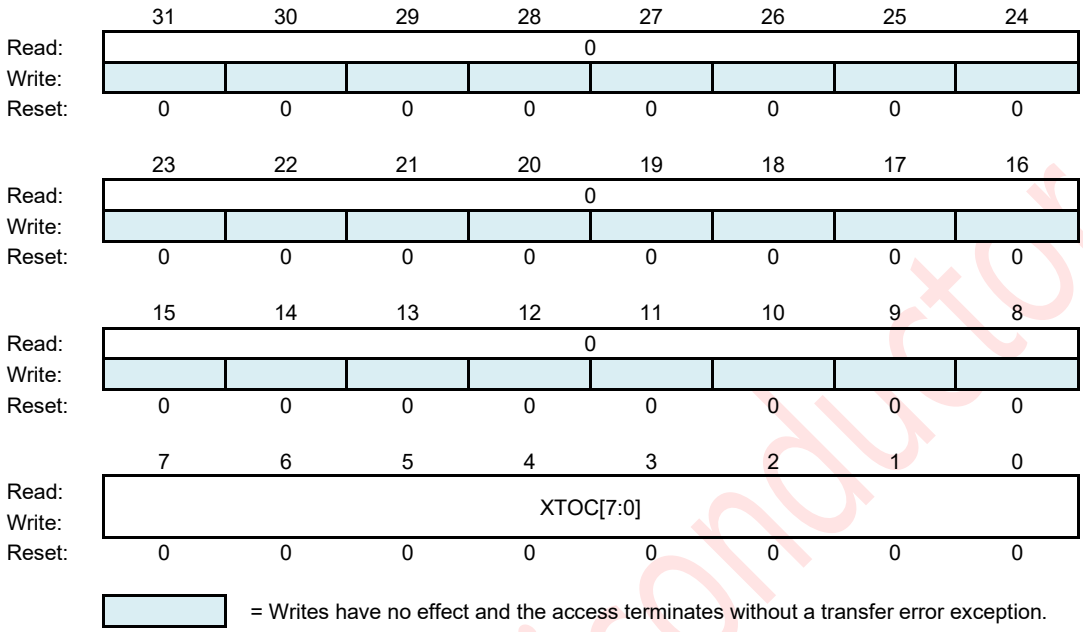


Figure 21-35: **XIP Continus Transfer Time Out Register (XIPCTTOR)**

XIP count down register for continuous mode. The counter is used to de-select the slave during continuous transfer mode. It is not possible to write to this register when the SSI is enabled (SSIC_EN = 1). The SSI is enabled and disabled by writing to the SSIENR register.

XTOC[7:0] — XIP time out value in terms of hclk.

Once slave is selected in continuous XIP mode this counter will be used to de-select the slave if there is no request for the time specified in the counter.

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21.7. Functional Description

21.7.1. Master Mode

This mode enables serial communication with serial -slave peripheral devices. When configured as a serial-master device, the SSI initiates and controls all serial transfers. **Figure 21-36** shows an example of the SSI configured as a serial master with all other devices on the serial bus configured as serial slaves.

The serial bit-rate clock, generated and controlled by the SSI, is driven out on the sclk_out line. When the SSI is disabled (SSIC_EN = 0), no serial transfers can occur and sclk_out is held in “inactive” state, as defined by the serial protocol under which it operates.

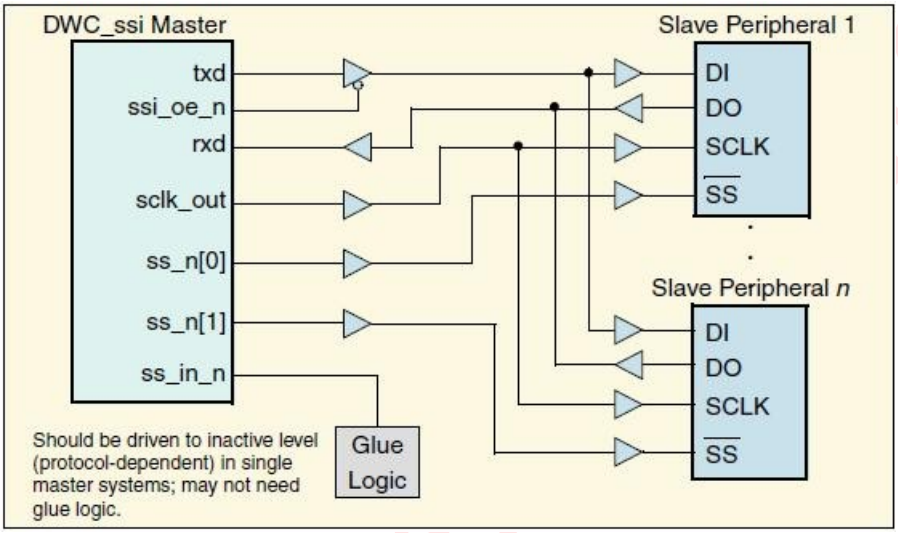


Figure 21-36: SSI Configured as Master Device

21.7.2. Clock Ratios

SSI works on an oversampling architecture. For the master mode of operation, the peripheral clock (sclk_out) period is a multiple of the internal core clock (ssi_clk).

When the SSI macrocell is configured as a master device, the maximum frequency of the bit-rate clock (sclk_out) is one-half the frequency of ssi_clk. This is to allow the shift control logic to capture data on one clock edge of sclk_out and propagate data on the opposite edge.

The frequency of sclk_out can be derived from the following equation.

$$F_{sclk_out} = \frac{F_{ssi_clk}}{SCKDV}$$

SCKDV is a programmable register holding any even value in the range 0 – 65,534. If SCKDV = 0, sclk_out is disabled.

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21.7.3. Receive and Transmit FIFO Buffers

The FIFO buffers used by the SSI are internal D-type flip-flops. The widths of both transmit and receive FIFO buffers are fixed at 32-bits due to the serial specifications, which state that a serial transfer (data frame) can be 4 to 32-bits in length. Data frames that are less than 32-bits in size must be right-justified when written into the transmit FIFO buffer. The shift control logic automatically right-justifies receive data in the receive FIFO buffer.

21.7.3.1. Transmit FIFO

The transmit FIFO is loaded by AHB write commands to the SSI data register (DR). Data are popped (removed) from the transmit FIFO by the shift control logic into the transmit shift register. The transmit FIFO generates a FIFO empty interrupt request (ssi_txe_intr) when the number of entries in the FIFO is less than or equal to the FIFO threshold value. The threshold value, set through the programmable register TXFTLR, determines the level of FIFO entries at which an interrupt is generated. The threshold value allows you to provide early indication to the processor that the transmit FIFO is nearly empty. A transmit FIFO overflow interrupt (ssi_txo_intr) is generated if you attempt to write data into an already full transmit FIFO.

21.7.3.2. Receive FIFO

Data are popped from the receive FIFO by AHB read commands to the SSI data register (DR). The receive FIFO is loaded from the receive shift register by the shift control logic. The receive FIFO generates a FIFO-full interrupt request (ssi_rxf_intr) when the number of entries in the FIFO is greater than or equal to the FIFO threshold value plus 1. The threshold value, set through programmable register RXFTLR, determines the level of FIFO entries at which an interrupt is generated.

The threshold value allows you to provide early indication to the processor that the receive FIFO is nearly full. A receive FIFO overrun interrupt (ssi_rxo_intr) is generated when the receive shift logic attempts to load data into a completely full receive FIFO. However, this newly received data are lost. A receive FIFO underflow interrupt (ssi_rxu_intr) is generated if you attempt to read from an empty receive FIFO. This alerts the processor that the read data are invalid.

21.7.4. DMA Operation

The SSI has optional built-in DMA capability which can be selected at configuration time; it has a handshaking interface to a DMA Controller to request and control transfers. The AHB bus is used to perform the data transfer to or from the DMA. While the SSI DMA operation is designed in a generic way to fit any DMA controller as easily as possible, it is designed to work seamlessly, and best used. To enable the DMA Controller interface on the SSI, you must write the DMA Control Register (DMACR). Writing a 1 into the TDMAE bit field of DMACR register enables the SSI transmit handshaking interface. Writing a 1 into the RDMAE bit field of the DMACR register enables the SSI receive handshaking interface.

21.7.5. SSI Interrupts

The SSI interrupts are described as follows:

Transmit FIFO Empty Interrupt (ssi_txe_intr) – Set when the transmit FIFO is equal to or below its threshold value and requires service to prevent an under-run. The threshold value, set through a software-programmable register, determines the level of transmit FIFO entries at which an interrupt is generated. This interrupt is cleared by hardware when data are written into the transmit FIFO buffer, bringing it over the threshold level.

Transmit FIFO Overflow Interrupt (ssi_txo_intr) – Set when an AHB access attempts to write into the transmit FIFO after it has been completely filled. When set, data written from the AHB is discarded. This interrupt remains set until you read the transmit FIFO overflow interrupt clear register (TXOICR).

Receive FIFO Full Interrupt (ssi_rxf_intr) – Set when the receive FIFO is equal to or above its threshold value plus 1 and requires service to prevent an overflow. The threshold value, set through a software-programmable register, determines the level of receive FIFO entries at which an interrupt is generated. This interrupt is cleared by hardware when data are read from the receive FIFO buffer, bringing it below the threshold level.

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Receive FIFO Overflow Interrupt (ssi_rxo_intr) – Set when the receive logic attempts to place data into the receive FIFO after it has been completely filled. When set, newly received data are discarded. This interrupt remains set until you read the receive FIFO overflow interrupt clear register (RXOICR).

Receive FIFO Underflow Interrupt (ssi_rxu_intr) – Set when an AHB access attempts to read from the receive FIFO when it is empty. When set, zeros are read back from the receive FIFO. This interrupt remains set until you read the receive FIFO underflow interrupt clear register (RXUICR).

Combined Interrupt Request (ssi_intr) – OR'ed result of all the above interrupt requests after masking. To mask this interrupt signal, you must mask all other SSI interrupt requests.

21.7.6. Enhanced SPI Modes

SSI supports the dual, quad, and octal modes of SPI using the SSIC_SPI_MODE configuration parameter. The possible values for this parameter are Standard, Dual SPI, Quad SPI and Octal SPI modes. When dual, quad, or octal mode is selected for this parameter, the width of TXD, RXD and ssi_oe_n signals change to 2, 4, or 8, respectively. Hence, the data is shifted out/in on more than one line, increasing the overall throughput. Dual SPI, Quad or Octal SPI modes function similarly except for the width of TXD, RXD and ssi_oe_n signals. The mode of operation (write/read) can be selected using the CTRLR0.TMOD field.

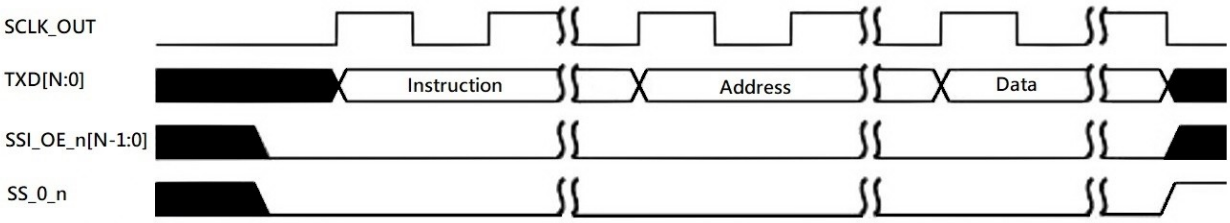


Figure 21-37: Typical Write Operation Dual/Quad/Octal SPI Mode

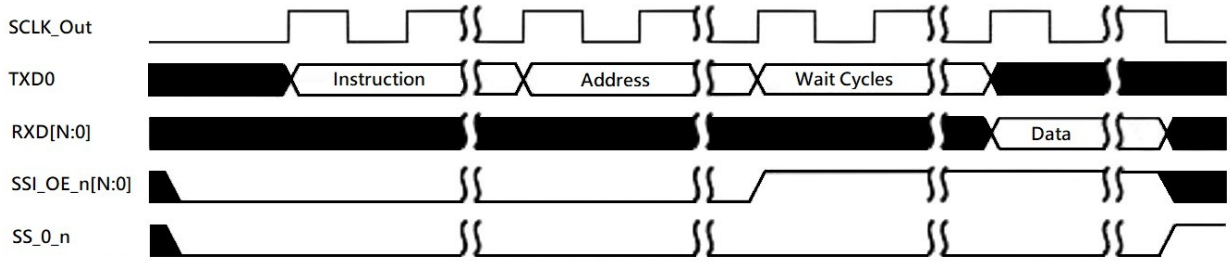


Figure 21-38: Typical Read Operation Dual/Quad/Octal SPI Mode

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21.7.7. Execute In Place (XIP) Mode

SSI provides a function to directly perform memory read operation from AHB transaction. This is called execute in place mode, in which SSI acts as memory mapped interface to an SPI memory. The XIP mode can be enabled in SSI by selecting the configuration parameter SSIC_XIP_EN. This includes an extra sideband signal xip_en on an AHB interface. This signal level decides if the AHB transfers are register read-write or XIP reads. Only AHB READs are supported during XIP operation. If xip_en signal is driven to 1, then SSI expects a read request to be made on the AHB interface. This request is translated to SPI read on the serial interface. As soon as the data is received, it is returned to AHB interface in same transaction. haddr is used to derive the address to be sent on the SPI interface. Certain devices expect the instruction phase to exist during XIP transfers. SSI supports inclusion of some fixed instruction sets during the XIP mode of operation.

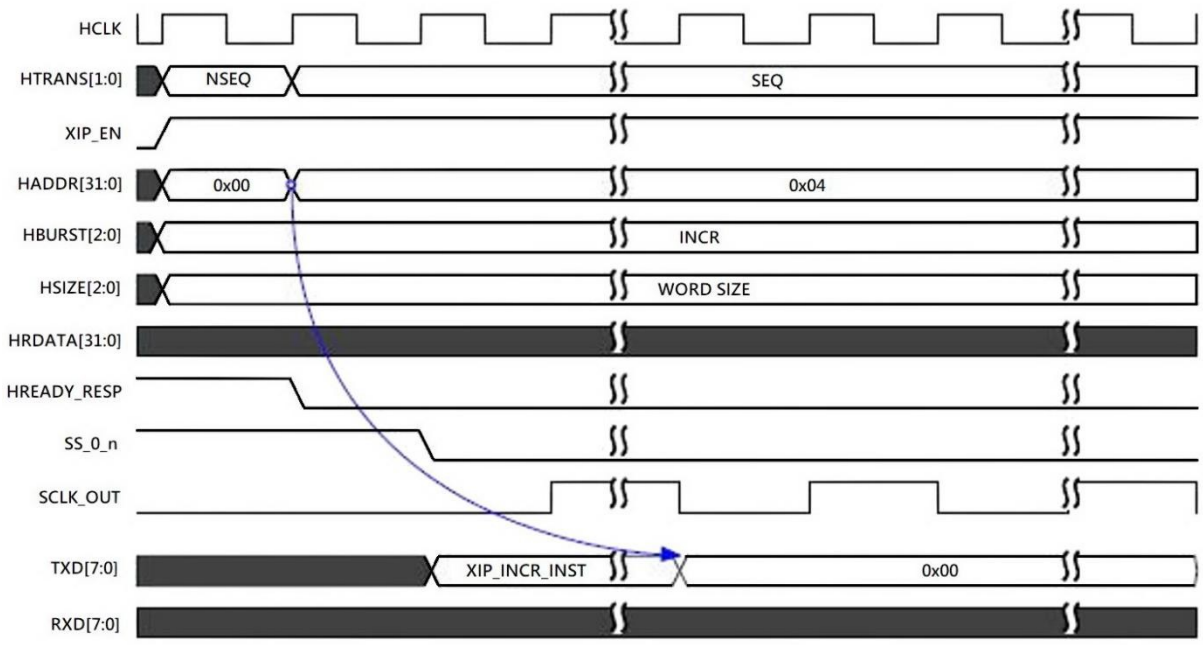


Figure 21-39: XIP Transfer with Instruction Phase

21.7.8. Continuous Transfer Mode in XIP

When SSI receives an XIP request, address from the AHB interface is transmitted onto the SPI interface directly . Each new transfer (XIP Read) on the AHB interface is treated in the same manner. Therefore, for every request, a new address must be sent to the device thereby contributing to the latency of the system.

If a memory device allows the stretching of slave select signal in between the XIP read transfers, then SSI can be programmed for continuous XIP mode to achieve higher performance. In this mode, the host fuses two or more AHB burst requests into a single SPI command by ensuring that the command and address are not retransmitted and the host controller need not wait for any dummy cycles in between these bursts.

When this function is enabled, then SSI functions in continuous XIP mode as soon as first XIP command is received. For the first XIP transfer, the address is sent on the SPI interface. After reception of requested data, SSI continues to keep the slave selected and the clock (sclk_out) remains in the default state. For subsequent XIP transfers on the AHB interface, SSI resumes the clock (sclk_out) and neither the command nor the address is transmitted onto the SPI interface and the data to be fetched from the device immediately (no dummy cycles).

- An undefined INCR (hburst = 001) burst is not supported in continuous read mode.

During the continuous transfer, a lot of power is dissipated on the slave device since the slave is selected all the times. To avoid such condition, SSI provides a configuration option to enable a watchdog timer to de-select the slave after the counter runs out.

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SSI can de-select the slave under the following conditions:

- A non-XIP command is received on an XIP interface (effectively any AHB transaction with xip_en driven to 0).
- When the AHB transaction is to a non-consecutive address, the slave select is removed and then SSI initiates a new XIP request.
- SSI does not detect any XIP transfer on AHB interface for the time-period specified in XIP_CNT_TIME_OUT register.

21.7.9. Data Pre-fetch in XIP Operations

Using the data pre-fetch feature in SSI, the controller pre-fetches the data for the successive burst during the current XIP transaction. If the next transaction request is made to the successive address, the data can be read directly from the RX FIFO instead of waiting for a new address and data to be sent to the device. This improves the overall performance of the system.

The amount of the data to be pre-fetched should be equal to the burst length of the last AHB request or the FIFO depth (whichever is lower). For example, if AHB defines a burst length of 16 starting from address 0x00, then SSI fetches 16 beats to complete the current transfer, and then again 16 more data frames will be fetched and kept into the data register. If AHB bus again requests for data starting from end address for last transfer, then the rest of the data will be sent to the device from RX FIFO itself. In parallel, SSI again starts an XIP transfer to the device to pre-fetch the next chunk of data. If AHB master does not define the contiguous address, then current data is flushed out from the FIFO and the controller starts a fresh transaction.

When SSI completes the current burst, and is pre-fetching the data for the next burst, a new XIP request may be placed. In this case, SSI can terminate the current transfer, or increase the number to data beats to be fetched depending on the address.

- If XIP pre-fetching is enabled, AHB request for incremental transfer of undefined length (hburst = 3'b001) is not allowed.

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22. Pulse Width Modulator (PWM)

22.1. Introduction

LT7589 has 4 PWM-Timers embedded. The 4 PWM-Timers has 2 Pre-scale, 2 clock divider, 4 clock selectors, 4 16-bits counters, 4 16-bits comparators, and 2 Dead-Zone generators. Each can be used as a timer and issue interrupt independently.

Each two PWM-Timers share the same pre-scale. Clock divider provides each timer with 5 clock sources (1, 1/2, 1/4, 1/8, 1/16). The 16-bits counter in each timer receives clock signal from clock selector and can be used to handle one PWM period. The 16-bits comparator compares number in counter with threshold number in register loaded previously to generate PWM duty cycle. The clock signal from clock divider is called PWM clock. Dead-Zone generator utilizes PWM clock as the clock source. Once Dead-Zone generator is enabled, the outputs of two PWM-Timers are blocked. Two output pins are all used as Dead-Zone generator output signals to control off-chip power device. The value of comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

Each PWM-Timer includes a capture channel. The Capture 0 and PWM 0 share a timer that is included in PWM 0; and the Capture 1 and PWM 1 share another timer, and etc. Therefore users must setup the PWM-Timer before turnning on Capture feature. After enabling capture feature, the capture always latched PWM-counter to CRLR when input channel has a rising transition and latched PWM-counter to CFLR when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0[1] (Rising latch Interrupt enable) and CCR0[2] (Falling latch Interrupt enable) to decide the interrupt trigger condition. Capture channel1&2&3 have the same feature. Whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reloaded at this moment. The maximal capture frequency should be decided by interrupt process time. If interrupt process time is T0, then the capture channel input signal should not change in T0, the maximal capture frequency is 1/T0.

There are only four interrupts from PWM to interrupt controller (INTC). PWM 0 and Capture 0 share the same interrupt; PWM1 and Capture 1 share the same interrupt and so on. Therefore, PWM function and Capture function in the same channel cannot be used at the same time.

22.2. Features

The Pulse Width Modulator includes below distinctive features:

- Programmable Period
- Programmable Duty Cycle
- Two Dead-Zone Generator
- Capture Function
- Pins can be configured as General-Purpose I/O

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22.3. Block Diagram

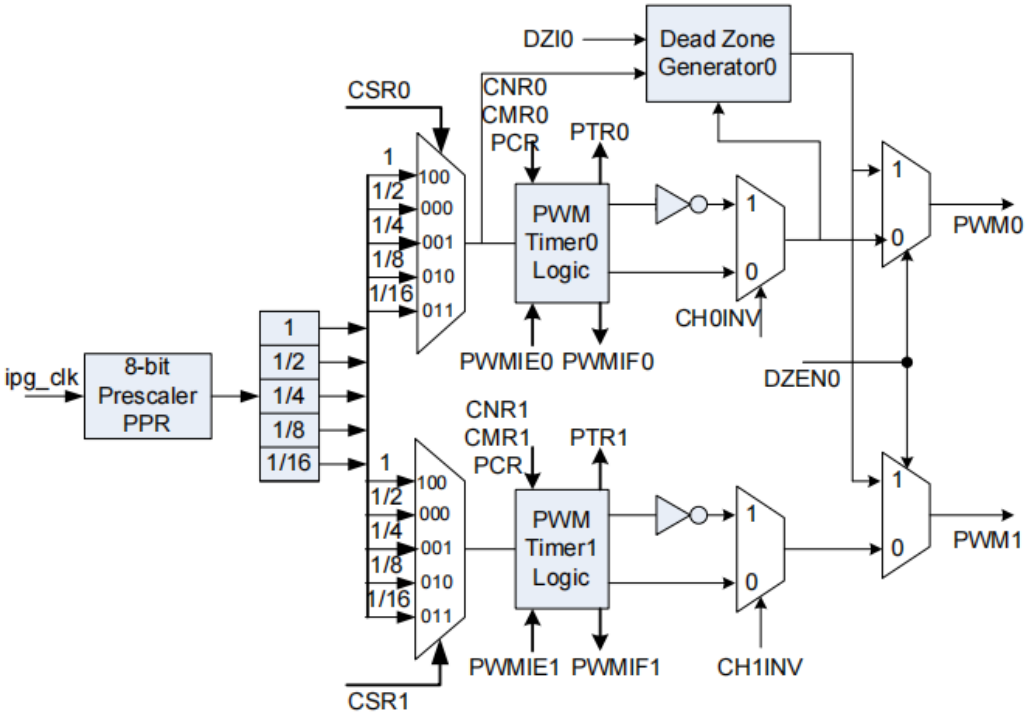


Figure 22-1: PWM Block Diagram

22.4. Signal Description

Table 22-1: PWM Signal Description

Name	I/O	Width	Reset State	Description
PWM0	I/O	1	0	PWM0 pin
PWM1	I/O	1	0	PWM1 pin
PWM2	I/O	1	0	PWM2 pin
PWM3	I/O	1	0	PWM3 pin

PWMx are used as a general-purpose input/output, and also used as the PWM send output or capture input.

In default state, it is used as general-purpose input port.

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22.5. Memory Map and Registers

The PWM Module memory map is shown in **Table 22-2**. The PWM0 base address is 0x400D_0000, and PWM1 is 0x400E_0000. This subsection describes the memory map and register structure of PWM.

22.5.1. Memory Map

Table 22-2: Module Memory Map

Address	Bit[31:0]	Access(1)
0x0000	PWM Pre-scale Register (PPR)	S/U
0x0004	PWM Clock Select Register (PCSR)	S/U
0x0008	PWM Control Register (PCR)	S/U
0x000C	PWM Counter Register0 (PCNR0)	S/U
0x0010	PWM Comparator Register0 (PCMR0)	S/U
0x0014	PWM Timer Register0 (PTR0)	S/U
0x0018	PWM Counter Register1 (PCNR1)	S/U
0x001C	PWM Comparator Register1 (PCMR1)	S/U
0x0020	PWM Timer Register1 (PTR1)	S/U
0x0024	PWM Counter Register2 (PCNR2)	S/U
0x0028	PWM Comparator Register2 (PCMR2)	S/U
0x002C	PWM Timer Register2 (PTR2)	S/U
0x0030	PWM Counter Register3 (PCNR3)	S/U
0x0034	PWM Comparator Register3 (PCMR3)	S/U
0x0038	PWM Timer Register3 (PTR3)	S/U
0x003C	PWM Interrupt Enable Register (PIER)	S/U
0x0040	PWM Interrupt Flag Register (PIFR)	S/U
0x0044	PWM Capture Control Register0 (PCCR0)	S/U
0x0048	PWM Capture Control Register1 (PCCR1)	S/U
0x004C	PWM Capture Rising Latch Register0 (PCRLR0)	S/U
0x0050	PWM Capture Falling Latch Register0 (PCFLR0)	S/U
0x0054	PWM Capture Rising Latch Register1 (PCRLR1)	S/U
0x0058	PWM Capture Falling Latch Register1 (PCFLR1)	S/U
0x005C	PWM Capture Rising Latch Register2 (PCRLR2)	S/U
0x0060	PWM Capture Falling Latch Register2 (PCFLR2)	S/U
0x0064	PWM Capture Rising Latch Register3 (PCRLR3)	S/U
0x0068	PWM Capture Falling Latch Register3 (PCFLR3)	S/U
0x006C	PWM Port Control Register (PPCR)	S/U

Note (1) : S/U = CPU supervisor or user mode access.

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22.5.2. Register Descriptions

22.5.2.1. PWM Pre-scale Register (PPR)

The register*(PPR)* is used to set prescaler and set dead zone length.

Address: PWMn_BASEADDR+0x0000_0000

	31	30	29	28	27	26	25	24
Read: Write:	DZI1[7:0]							
Reset:	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
Read: Write:	DZI0[7:0]							
Reset:	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
Read: Write:	CP1[7:0]							
Reset:	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
Read: Write:	CP0[7:0]							
Reset:	0	0	0	0	0	0	0	0

Figure 22-2: PWM Pre-scale Register (PPR)

DZI1[7:0] — Dead zone interval register 1 for PWM2 and PWM3

These 8-bits determine dead zone length. The 1 unit time of dead zone length is received from clock selector 1.

DZI0[7:0] — Dead zone interval register 0 for PWM0 and PWM1

These 8-bits determine dead zone length. The 1 unit time of dead zone length is received from clock selector 0.

CP1[7:0] — Clock pre-scale 1 for PWM Timer 2 & 3

Clock input is divided by (CP1 + 1) before it is fed to the counter of PWM Timer 2 & 3.

CP0[7:0] — Clock pre-scale 0 for PWM Timer 0 & 1

Clock input is divided by (CP0 + 1) before it is fed to the counter of PWM Timer 0 & 1.

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22.5.2.2. PWM Clock Select Register (PCSR)

Clock divider provides each timer with 5 clock sources (1, 1/2, 1/4, 1/8, 1/16). Each timer receives its own clock signal from clock divider which receives clock from 8-bits pre-scale.

Address: PWMn_BASEADDR+0x0000_0004

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0	CSR3[2:0]			0	CSR2[2:0]		
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0	CSR1[2:0]			0	CSR0[2:0]		
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-3: PWM Clock Select Register(PCSR)

CSR3[2:0] — Timer 3 Clock Source Selection
Select clock input for timer 3.

Table 22-3: Timer 3 Clock Source Selection

CSR3[2:0]	Input Clock Divided by
100~111	1
011	16
010	8
001	4
000	2

CSR2[2:0] — Timer 2 Clock Source Selection
Select clock input for timer 2. Same as CSR3.

CSR1[2:0] — Timer 1 Clock Source Selection
Select clock input for timer 1. Same as CSR3.

CSR0[2:0] — Timer 0 Clock Source Selection
Select clock input for timer 0. Same as CSR3.

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22.5.2.3. PWM Control Register (PCR)

This register is the PWM control register.

Address: PWMn_BASEADDR+0x0000_0008

	31	30	29	28	27	26	25	24
Read:	0				CH3MOD	CH3INV	0	CH3EN
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0				CH2MOD	CH2INV	0	CH2EN
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0				CH1MOD	CH1INV	0	CH1EN
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0		DZEN1	DZEN0	CH0MOD	CH0INV	0	CH0EN
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-4: PWM Control Register (PCR)

CH3MOD — Timer 3 Auto-load/One-Shot Mode

1 = Auto-load Mode

0 = One-Shot Mode

Note: If there is a rising or falling transition at this bit, it will cause CNR3 and CMR3 to be cleared.

CH3INV — Timer 3 Inverter ON/OFF

1 = Inverter ON

0 = Inverter OFF

CH3EN — Timer 3 Enable/Disable

1 = Enable

0 = Disable

CH2MOD — Timer 2 Auto-load/One-Shot Mode

1 = Auto-load Mode

0 = One-Shot Mode

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Note: If there is a rising or falling transition at this bit, it will cause CNR2 and CMR2 to be cleared.

CH2INV — Timer 2 Inverter ON/OFF

1 = Inverter ON

0 = Inverter OFF

CH2EN — Timer 2 Enable/Disable

1 = Enable

0 = Disable

CH1MOD — Timer 1 Auto-load/One-Shot Mode

1 = Auto-load Mode

0 = One-Shot Mode

Note: If there is a rising or falling transition at this bit, it will cause CNR1 and CMR1 to be cleared.

CH1INV — Timer 1 Inverter ON/OFF

1 = Inverter ON

0 = Inverter OFF

CH1EN — Timer 1 Enable/Disable

1 = Enable

0 = Disable

DZEN1 — Dead-Zone 1 Generator Enable/Disable

1 = Enable

0 = Disable

Note: When DZEN1 is enabled, CH3EN should be disabled. Because channel3 and channel2 outputs are both decided by channel2.

DZEN0 — Dead-Zone 0 Generator Enable/Disable

1 = Enable

0 = Disable

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Note: When DZEN0 is enabled, CH1EN should be disabled. Because channel1 and channel0 outputs are both decided by channel0.

CH0MOD — Timer 0 Auto-load/One-Shot Mode

1 = Auto-load Mode

0 = One-Shot Mode

Note: If there is a rising or falling transition at this bit, it will cause CNR0 and CMR0 to be cleared.

CH0INV — Timer 0 Inverter ON/OFF

1 = Inverter ON

0 = Inverter OFF

CH0EN — Timer 0 Enable/Disable

1 = Enable

0 = Disable

22.5.2.4. PWM Counter Register (PCNRn)

These registers control the period of the PWM by defining the number of the count_pulse in the period.

Address: PWMn_BASEADDR+0x0000_000C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CNR0[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CNR0[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

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Address: PWMn_BASEADDR+0x0000_0018

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CNR1[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CNR1[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Address: PWMn_BASEADDR+0x0000_0024

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CNR2[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CNR2[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

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Address: PWMn_BASEADDR+0x0000_0030

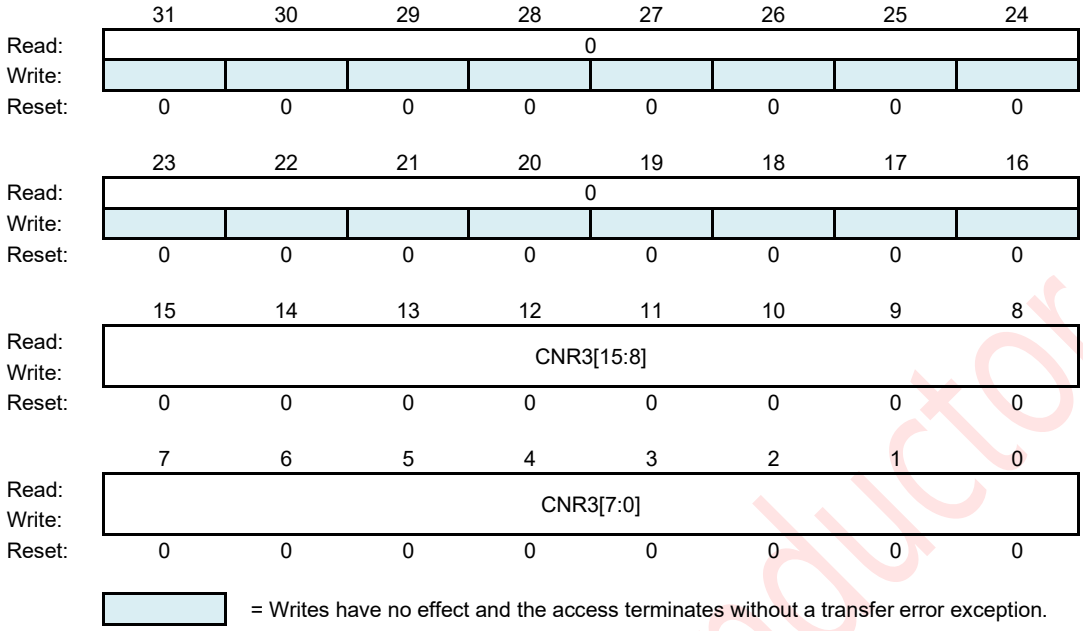


Figure 22-5: PWM Counter Register (PCNR)

CNRx[15:0] — Loaded Value for PWM Counter/Timer
Data range: 65535~0 (Unit: 1 PWM clock cycle)

Note:

1: One PWM cycle width = CNR + 1. If CNR equal zero, PWM counter/timer will be stopped.

2: Whenever a value is written to CNR, it will take effect in the next PWM Counter cycle.

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22.5.2.5. PWM Comparator Register (PCMRn)

These registers define the width of the pulse. When the counter matches the value in this register, the output is reset for the duration of the period.

Address: PWMn_BASEADDR+0x0000_0010

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CMR0[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CMR0[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Address: PWMn_BASEADDR+0x0000_001C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CMR1[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CMR1[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

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Address: PWMn_BASEADDR+0x0000_0028

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CMR2[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CMR2[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Address: PWMn_BASEADDR+0x0000_0034

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CMR3[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CMR3[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-6: **PWM Comparator Register (PCMR)**

CMRx[15:0] — PWM Comparator Register
Data range: 65535~0 (Unit: 1 PWM clock cycle)

CMR are used to determine PWM output duty ratio.
Assumption: PWM output initial: high

CMR >= CNR : PWM output is always high
CMR < CNR : PWM output high = (CMR + 1) unit
CMR = 0 : PWM output high = 1 unit

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Note:

1: PWM duty = CMR + 1. If CMR equals zero, PWM duty = 1

2: Whenever a value is written to CMR, it will take effect in the next PWM Counter cycle.

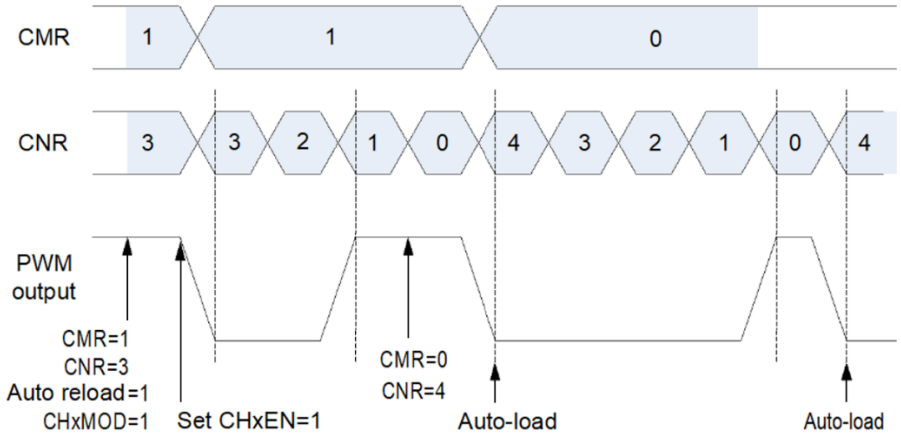


Figure 22-7: **PWM Output**

Modulate PWM Controller output duty ratio (CNR = 150)

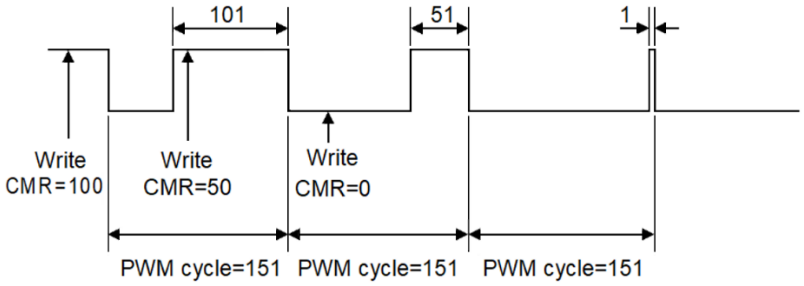


Figure 22-8: **PWM Duty Cycle**

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22.5.2.6. PWM Timer Register (PTRn)

The read-only PWM timer registers hold the current count value. It can be read at any time without disturbing the counter.

Address: PWMn_BASEADDR+0x0000_0014

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	PTR0[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	PTR0[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Address: PWMn_BASEADDR+0x0000_0020

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	PTR1[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	PTR1[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

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Address: PWMn_BASEADDR+0x0000_002C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	PTR2[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	PTR2[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Address: PWMn_BASEADDR+0x0000_0038

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	PTR3[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	PTR3[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-9: PWM Timer Register (PTR)

PTRx[15:0] — PWM Timer value

The read-only PTR bits holds the current count value. Users can monitor PTR to obtain the current value in the 16-bits down counter.

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22.5.2.7. PWM Interrupt Enable Register (PIER)

This register is used to enable PWM timer interrupt.

Address: PWMn_BASEADDR+0x0000_003C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0				PIER3	PIER2	PIER1	PIER0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-10: PWM Interrupt Enable Register (PIER)

PIER3 — PWM Timer 3 Interrupt Enable
1 = Enable
0 = Disable

PIER2 — PWM Timer 2 Interrupt Enable
1 = Enable
0 = Disable

PIER1 — PWM Timer 1 Interrupt Enable
1 = Enable
0 = Disable

PIER0 — PWM Timer 0 Interrupt Enable
1 = Enable
0 = Disable

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22.5.2.8. PWM Interrupt Flag Register (PIFR)

This register is used to indicate PWM timer interrupt flag.

Address: PWMn_BASEADDR+0x0000_0040

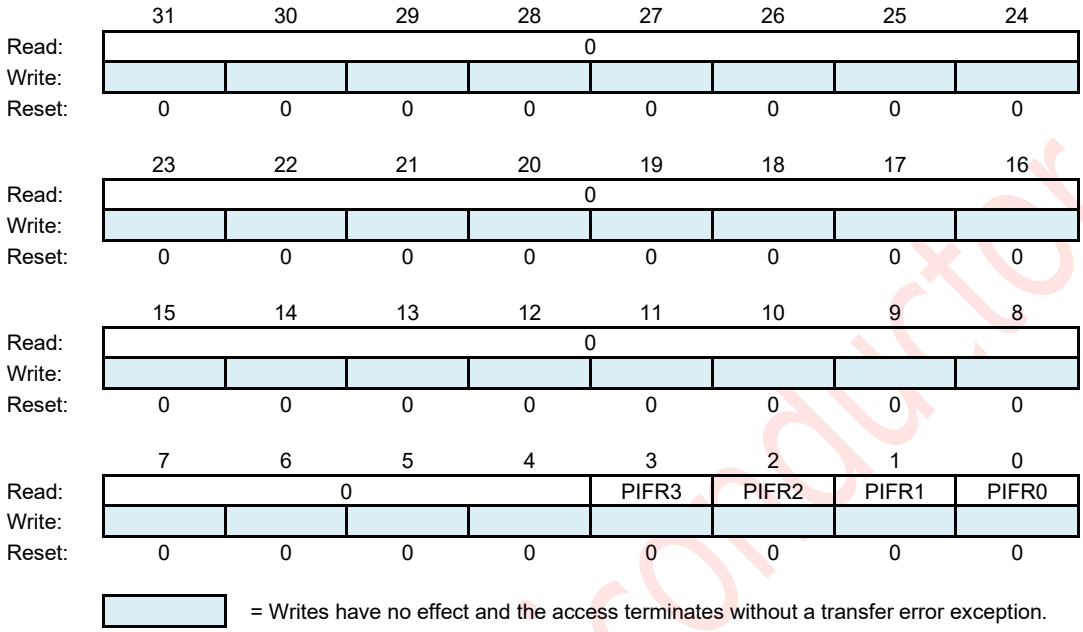


Figure 22-11: PWM Interrupt Flag Register (PIFR)

PIFR3 — PWM Timer 3 Interrupt Flag.
When PWM timer3 counts to 0, and PIER3 = 1, PIFR3 will be set to 1. Writing 1 to this bit will clear PIFR3.
1 = Interrupt Flag on
0 = Interrupt Flag off

PIFR2 — PWM Timer 2 Interrupt Flag.
When PWM timer2 counts to 0, and PIER2 = 1, PIFR2 will be set to 1. Writing 1 to this bit will clear PIFR2.
1 = Interrupt Flag on
0 = Interrupt Flag off

PIFR1 — PWM Timer 1 Interrupt Flag.
When PWM timer1 counts to 0, and PIER1 = 1, PIFR1 will be set to 1. Writing 1 to this bit will clear PIFR1.
1 = Interrupt Flag on
0 = Interrupt Flag off

PIFR0 — PWM Timer 0 Interrupt Flag.
When PWM timer0 counts to 0, and PIER0 = 1, PIFR0 will be set to 1. Writing 1 to this bit will clear PIFR0.
1 = Interrupt Flag on
0 = Interrupt Flag off

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22.5.2.9. PWM Capture Control Register (PCCR0/1)

These registers are used to control the capture function.

Address: PWMn_BASEADDR+0x0000_0044

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	CFLRD1	CRLRD1	0	CAPIF1	CAPCH1 EN	FL_IE1	RL_IE1	INV1
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CFLRD0	CRLRD0	0	CAPIF0	CAPCH0 EN	FL_IE0	RL_IE0	INV0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-12: PWM Capture Control Register (PCCR0)

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Address: PWMn_BASEADDR+0x0000_0048

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	CFLRD3	CRLRD3	0	CAPIF3	CAPCH3 EN	FL_IE3	RL_IE3	INV3
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CFLRD2	CRLRD2	0	CAPIF2	CAPCH2 EN	FL_IE2	RL_IE2	INV2
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-13: PWM Capture Control Register (PCCR1)

CFLRDx — Capture Falling Latch Register load flag

1 = When input channel x has a falling transition, CFLRx was updated and this bit was “1”.

0 = When input channel x does not have a falling transition.
write 1 to clear this bit.

CRLRDx — Capture Rising Latch Register load flag

1 = When input channel x has a rising transition, CRLRx was updated and this bit was “1”.

0 = When input channel x does not have a rising transition.

write 1 to clear this bit.

CAPIFx — Capture Channel x interrupt flag

1 = When input channel x has a falling transition, and FL_IEx bit is enabled, this interrupt flag will be set. When input channel x has a rising transition, and RL_IEx bit is enabled, this interrupt flag will also be set.

0 = Capture channel x interrupt flag is not set.

write 1 to clear this bit.

CAPCHxEN — Capture Channel x Enable/Disable

1 = Enable

0 = Disable

When this bit is set to 1, Capture latched the PMW-counter and the value is saved to CRLR (Rising latch) and CFLR (Falling latch). When this bit is set to 0, Capture does not update CRLR and CFLR, and disables Channel x Interrupt.

FL_IEx — Channel x Falling Interrupt Enable ON/OFF

1 = Enable

0 = Disable

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When this bit is set to 1, if Capture detects Channel x has a falling transition, Capture issues an Interrupt.

RL_IEx — Channel x Rising Interrupt Enable ON/OFF

1 = Enable

0 = Disable

When this bit is set to 1, if Capture detects Channel x has a rising transition, Capture issues an Interrupt.

INVx — Channel x Inverter ON/OFF

1 = Inverter ON

0 = Inverter OFF

22.5.2.10. PWM Capture Rising Latch Register (PCRLRn)

These registers are used to latch the PWM counter when capture rising transition.

Address: PWMn_BASEADDR+0x0000_004C

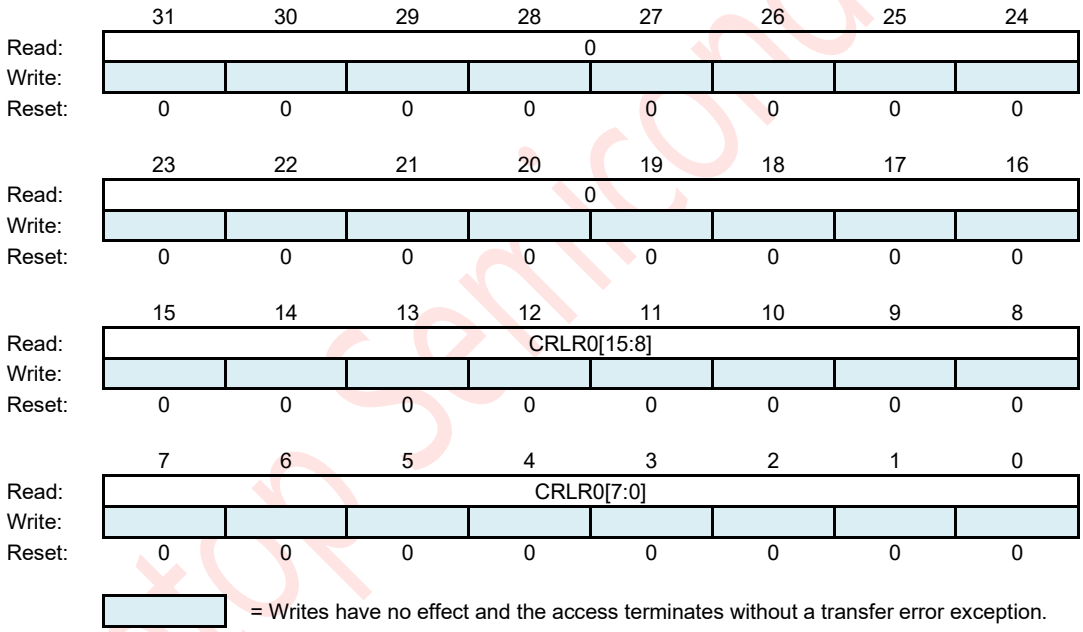


Figure 22-14: PWM Capture Rising Latch Register (PCRLR0)

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Address: PWMn_BASEADDR+0x0000_0054

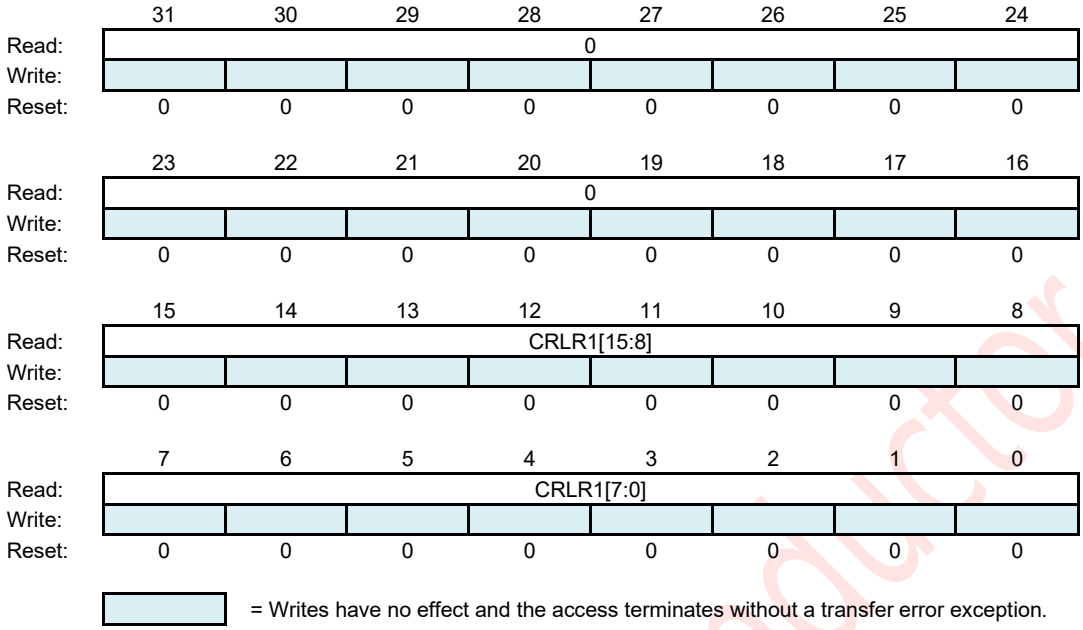


Figure 22-15: PWM Capture Rising Latch Register (PCRLR1)

Address: PWMn_BASEADDR+0x0000_005C

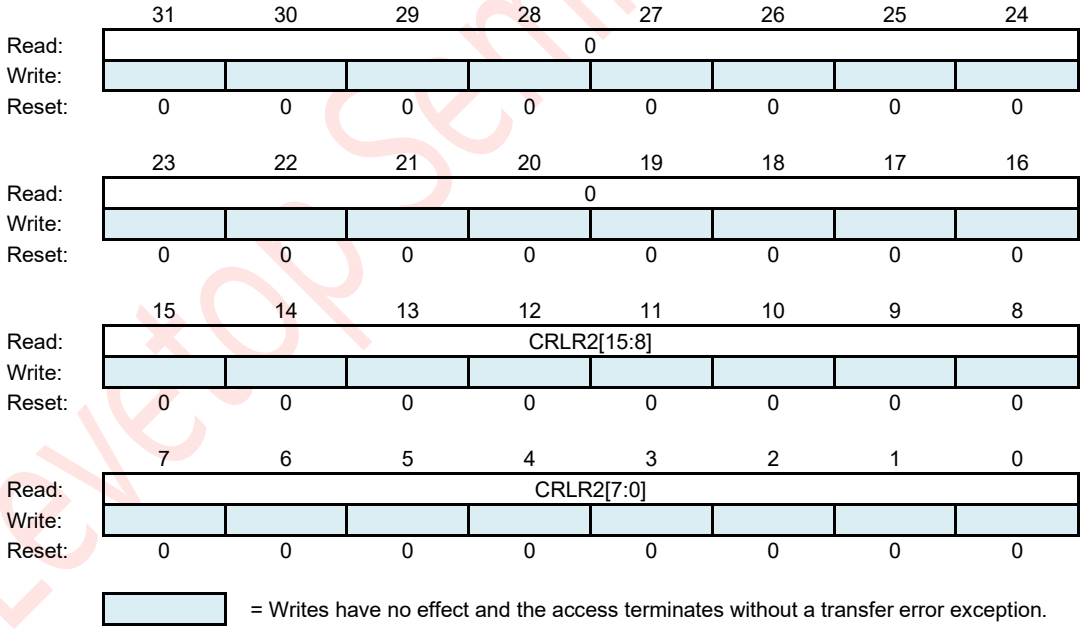


Figure 22-16: PWM Capture Rising Latch Register (PCRLR2)

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Address: PWMn_BASEADDR+0x0000_0064

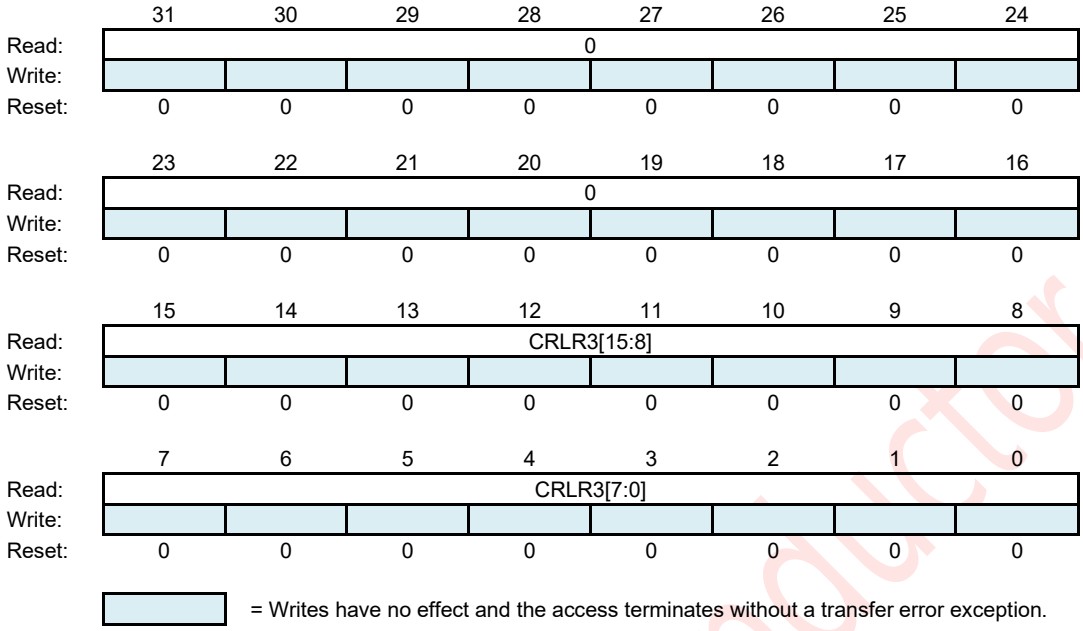


Figure 22-17: PWM Capture Rising Latch Register (PCRLR0/1/2/3)

CRLRx[15:0] — Capture Rising Latch Registerx

Latch the PWM counter when Channel x has a rising transition.

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22.5.2.11. PWM Capture Falling Latch Register (PCFLRn)

These registers are used to latch the PWM counter when a falling transition is captured.

Address: PWMn_BASEADDR+0x0000_0050

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CFLR0[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CFLR0[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-18: PWM Capture Falling Latch Register (PCFLR0)

Address: PWMn_BASEADDR+0x0000_0058

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	CFLR1[15:8]							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CFLR1[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 22-19: PWM Capture Falling Latch Register (PCFLR1)

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Address: PWMn_BASEADDR+0x0000_0060

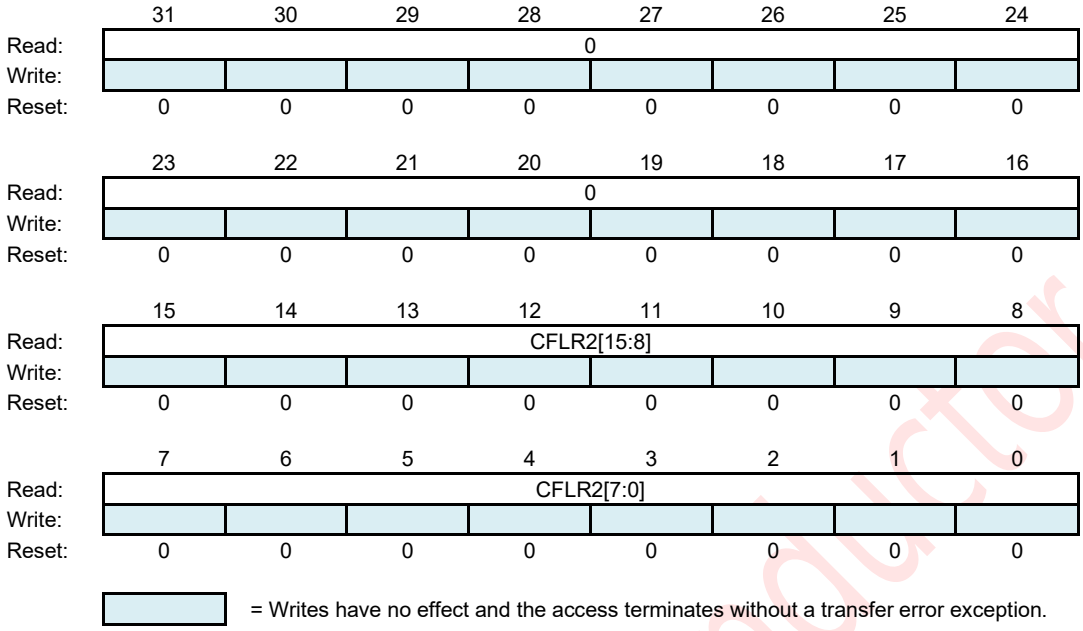


Figure 22-20: PWM Capture Falling Latch Register (PCFLR2)

Address: PWMn_BASEADDR+0x0000_0068

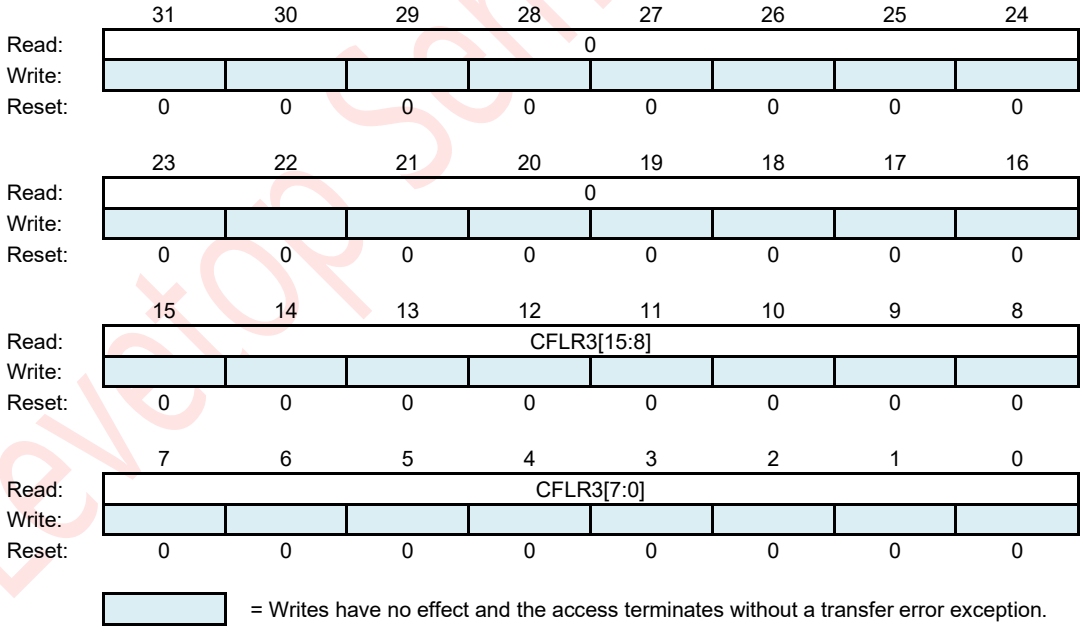


Figure 22-21: PWM Capture Falling Latch Register (PCFLR3)

CFLRx[15:0] — Capture Falling Latch Registerx

Latch the PWM counter when Channel x has a falling transition.

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22.5.2.12. PWM Port Control Register (PPCR)

The register(PPCR) is used to control PWMx pin direction and pin status.

Address: PWMn_BASEADDR+0x0000_006C

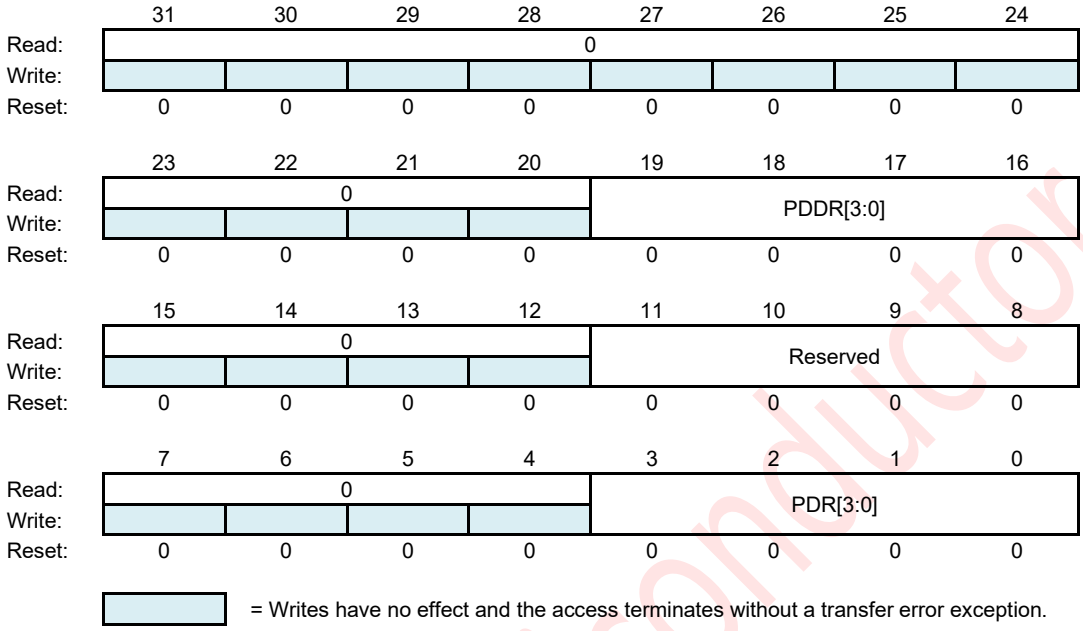


Figure 22-22: PWM Port Control Register (PPCR)

PDDR[3:0] — Port Data Direction Register

The PDDR[3:0] bits control the direction of PWM Pins. Reset clear PDDR[3:0].

1 = Corresponding pin is configured as output

0 = Corresponding pin is configured as input

PDR[3:0] — Port Data Register

Writing data to PDR[3:0] can drive corresponding pins that are configured as general-purpose outputs. Reading an input (PDDR bit clear) returns the pin level.

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22.6. Functional Descriptions

This subsection describes the PWM functional operation.

22.6.1. PWM Double Buffering And Automatic Reload

PWM-Timers have a double buffering function, enabling the reload value changed for next timer operation without stopping current timer operation. Although a new timer value is set, the current timer operation still operates successfully. The counter value can be written into CNR0~3 and the current counter value can be read from PTR0~3. The auto-reload operation will copy the data from CNR0~3 to the down-counter when the down-counter reaches zero. If CNR0~3 are set as zero, the counter will be halt when the counter count to zero. If auto-reload bit is set as zero, the counter will be stopped immediately.

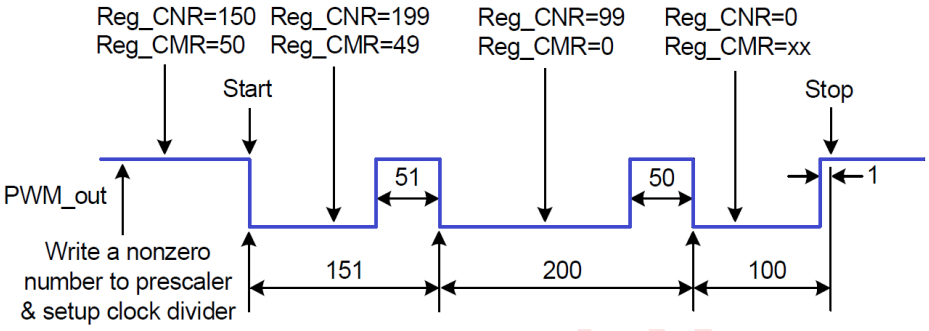


Figure 22-23: PWM Double Buffering Illustration

22.6.2. Modulate Duty Ratio

The double buffering function allows CMR to be written at any point in the current cycle. The loaded value will take effect from the next cycle.

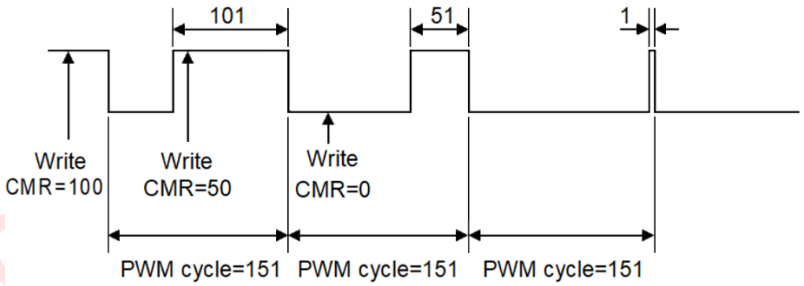


Figure 22-24: PWM Controller Output Duty Ratio

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22.6.3. Dead-Zone Generator

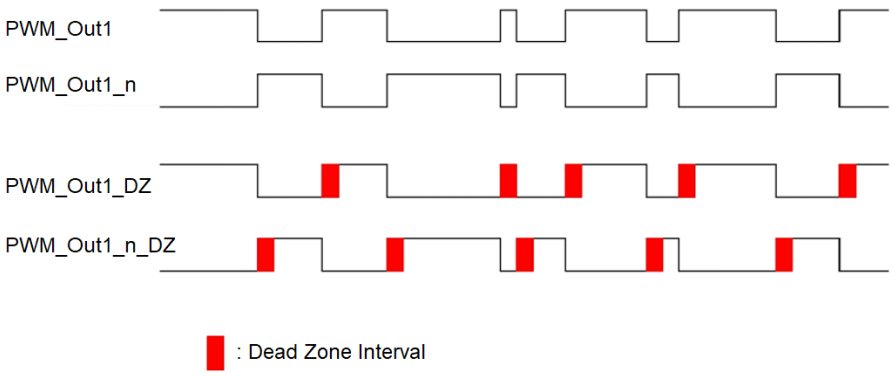


Figure 22-25: Dead Zone Generation Operation

22.6.4. PWM Timer Start Procedure

1. Setup clock selector (CSR)
2. Setup prescaler & dead zone interval (PPR)
3. Setup inverter on/off, dead zone generator on/off, toggle mode /one-shot mode, and PWM timer off. (PCR)
4. Setup the comparator register (CMR)
5. Setup the counter register (CNR)
6. Setup the interrupt enable register (PIER)
7. Setup PWMx as output pin (PPCR)
8. Enable PWM timer (PCR)

22.6.5. PWM Timer Stop Procedure

Method 1:
Set 16-bits down counter (CNR) as 0, and monitor PTR. When PTR reaches to 0, disable PWM timer (PCR). (Recommended)

Method 2:
Set 16-bits down counter (CNR) as 0. When an interrupt request happens, disable PWM timer (PCR). (Recommended)

Method 3:
Disable PWM timer directly (PCR). (Not recommended)

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22.6.6. Capture Start Procedure

1. Setup clock selector (CSR)
2. Setup pre-scale (PPR)
3. Setup inverter on/off, dead zone generator on/off, auto-load mode/one-shot mode, and PWM timer off. (PCR)
4. Setup the counter register (CNR)
5. Setup the capture register (CCR)
6. Setup PWMx as input pin (PPCR)
7. Enable PWM timer (PCR)

22.6.7. Capture Basic Timer Operation

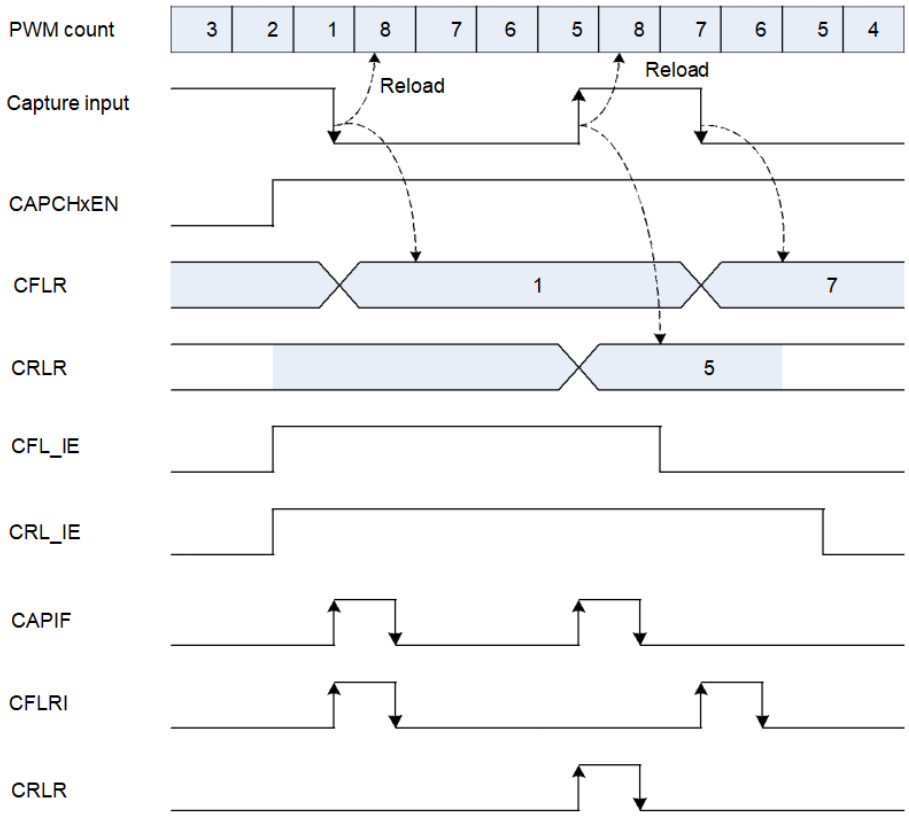


Figure 22-26: Capture Basic Timer Operation

At this case, the CNR is 8:

1. When CAPIFx is set to 1, the PWM counter CNRx will be reload.
2. The channel low pulse width is (CNR +1 – CRLR).
3. The channel high pulse width is (CNR +1 - CFLR).

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23. Analog Comparator (COMP)

23.1. Introduction

The Analog Comparator offers programmable response time, hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous “Filtered” output (CP), or an asynchronous “raw” output (CPA). The asynchronous CPA signal is available even when the system clock is not active. This allows the Comparator to operate and generate an output with the device in STOP mode.

23.2. Block Diagram

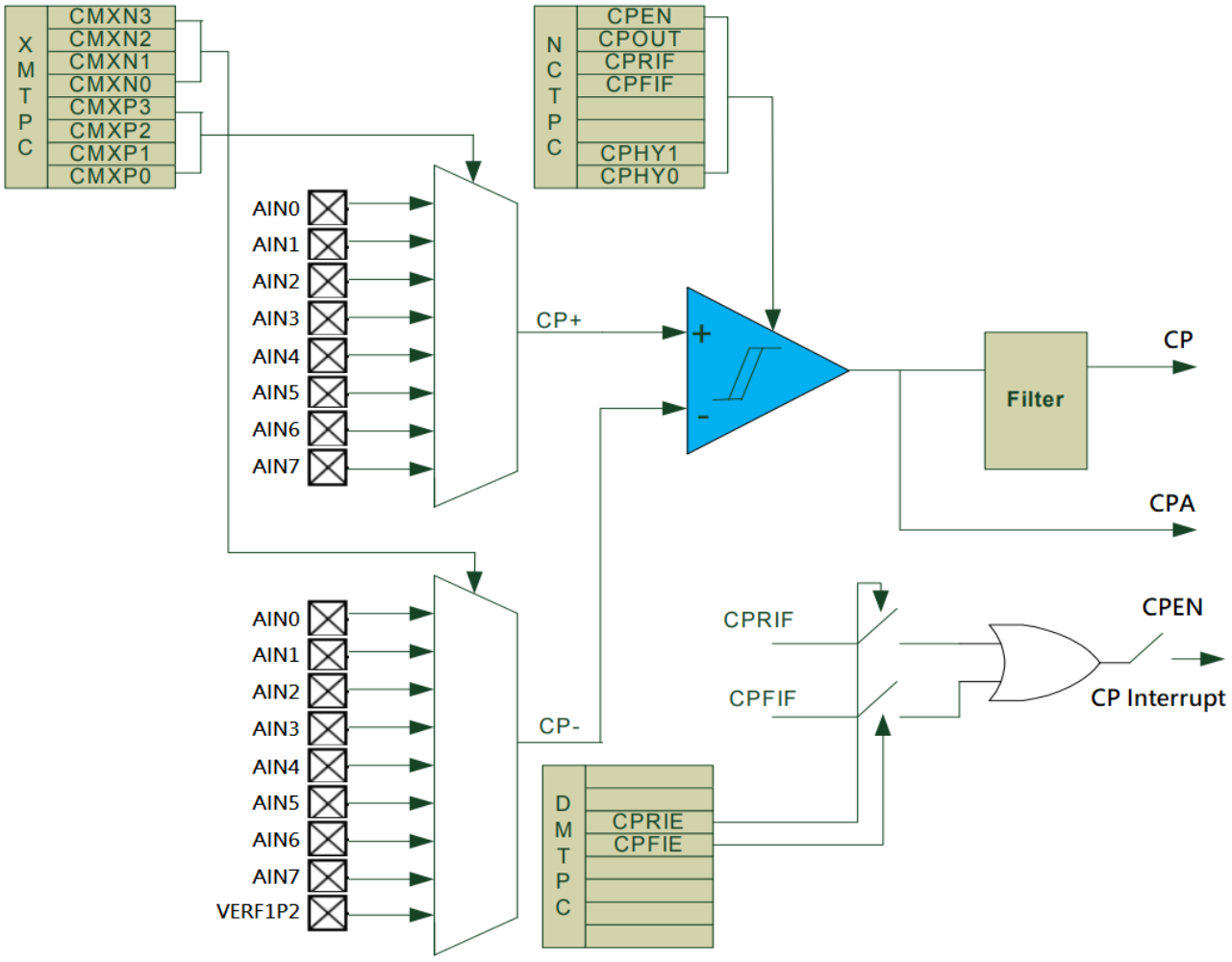


Figure 23-1: Comparator Block Diagram

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23.3. Modes of Operation

This subsection describes the three low-power modes.

23.3.1. Wait Mode

In wait mode, the Comparator module can continue to operate normally by setting CPEN bit and can be configured to exit the low-power mode by generating an interrupt request.

23.3.2. Doze Mode

In doze mode, the Comparator module can continue to operate normally by setting CPEN bit and can be configured to exit the low-power mode by generating an interrupt request.

23.3.3. Stop Mode

In stop mode, the system clock is absent, and the Comparator module can continue to operate normally by setting CPEN bit and can be configured to exit the low-power mode by generating an asynchronous “raw” output (CPA) wakeup signal.

23.4. Memory Map and Registers

The Comparator Module memory map is shown in **Table 23-1**. The COMP0 base address is 0x400A_0000, and COMP1 is 0x400B_0000. This subsection describes the memory map and register structure for Comparator.

23.4.1. Memory Map

Refer to **Table 23-1** for a description of the memory map.
This device has two Comparator modules.

Table 23-1: Comparator Module Memory Map

Offset Address	Bits[7:0]	Access(1)
0x3	Comparator Control Register(CPTCN)	S/U
0x2	Comparator0 Mode Selection Register(CPTMD)	S/U
0x1	Comparator MUX Selection Register(CPTMX)	S/U
0x0	Comparator Output Filter Selection Register(CPTFS)	S/U

Note (1) : S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. Accessing supervisor only address in user mode has no effect and result in a cycle termination transfer error.

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23.4.2. Register Descriptions

The Comparator programming model consists of below registers:

- •CPTCN: Comparator Control Register.
- •CPTMD: Comparator Mode Selection Register.
- •CPTMX: Comparator MUX Selection Register.
- •CPTFLS: Comparator Output Filter Selection Register

23.4.2.1. Comparator Control Register (CPTCN)

Address: COMP0_BASEADDR+0x0000_0003, COMP1_BASEADDR+0x0000_0003

	7	6	5	4	3	2	1	0
Read:	CPEN	CPOUT	CPRIF	CPFIF	0	0	CPHY[1:0]	
Write:								
Reset:	0	0	0	0	0	0	0	1

= Writes have no effect and the access terminates without a transfer error exception.

Figure 23-2: Comparator Control Register (CPTCN)

CPEN — Comparator Enable Bit

The read/write CPEN bit enables Comparator operation. When the Comparator is disabled, CPOUT is low state.

1 = Comparator is enabled

0 = Comparator is disabled

CPOUT — Comparator Output State Flag.

1 = Voltage on CP+ > CP–.

0 = Voltage on CP+ < CP–.

CPRIF — Comparator Rising-Edge Flag. Must be cleared by writing one to this bit.

1 = Comparator Rising Edge has occurred.

0 = No Comparator Rising Edge has occurred since this flag was last cleared.

CPFIF — Comparator Falling-Edge Flag. Must be cleared by writing one to this bit.

1 = Comparator Falling-Edge has occurred.

0 = No Comparator Falling-Edge has occurred since this flag was last cleared.

CPHY[1:0] — Comparator Hysteresis Control Bits.

00 = Hysteresis is disabled.

01 = Hysteresis = 8 mV.

10 = Hysteresis = 12 mV.

11 = Hysteresis = 15.4 mV.

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23.4.2.2. Comparator Mode Selection Register (CPTMD)

Address: COMP0_BASEADDR+0x0000_0002, COMP1_BASEADDR+0x0000_0002

	7	6	5	4	3	2	1	0
Read:	CPOEN	0	CPRIE	CPFIE	0	WKUPLEVEL	0	CPMD
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 23-3: Comparator Mode Selection Register(CPTMD)

CPOEN — Comparator Output to pad control bit.

1 = Comparator output can be observed in PWM1[0] for COMP0 and PWM1[1] for COMP1.

0 = Comparator output is disabled.

CPRIE — Comparator Rising-Edge Interrupt Enable.

1 = Comparator Rising-edge interrupt is enabled.

0 = Comparator Rising-edge interrupt is disabled.

CPFIE — Comparator Falling-Edge Interrupt Enable.

1 = Comparator Falling-edge interrupt is enabled.

0 = Comparator Falling-edge interrupt is disabled.

WKUPLEVEL — Comparator WakeUp level control bit.

1 = Voltage on CP+ > CP– will generate an wakeup request during stop mode.

0 = Voltage on CP+ < CP– will generate an wakeup request during stop mode.

CPMD — Comparator Mode Select. These bits select the response time for Comparator.

Table 23-2: Comparator Mode Selection

Mode	CPMD	Response Time	Power Consumption
Low-speed	0	500ns	3.3uA
High-speed	1	80ns	22uA

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23.4.2.3. Comparator MUX Selection Register (CPTMX)

Address: COMP0_BASEADDR+0x0000_0001, COMP1_BASEADDR+0x0000_0001

	7	6	5	4	3	2	1	0
Read: Write:	CMXN[3:0]				CMXP[3:0]			
Reset:	1	1	1	1	1	1	1	1

Figure 23-4: Comparator MUX Selection Register(CPTMX)

CMXN[3:0] — Comparator Negative Input MUX Select. These bits select which Port pin is used as the Comparator negative input.

Table 23-3: Comparator Negative Input MUX Selection

CMXN3	CMXN2	CMXN1	CMXN0	Negative Input
0	0	0	0	AIN0
0	0	0	1	AIN 1
0	0	1	0	AIN 2
0	0	1	1	AIN 3
0	1	0	0	AIN 4
0	1	0	1	AIN 5
0	1	1	0	AIN 6
0	1	1	1	AIN 7
1	0	0	0	Vref1p2
Other value				None

CMXP[3:0] — Comparator Positive Input MUX Select. These bits select which Port pin is used as the Comparator positive input.

Table 23-4: Comparator Positive Input MUX Selection

CMXP3	CMXP2	CMXP1	CMXP0	Positive Input
0	0	0	0	AIN0
0	0	0	1	AIN 1
0	0	1	0	AIN 2
0	0	1	1	AIN 3
0	1	0	0	AIN 4
0	1	0	1	AIN 5
0	1	1	0	AIN 6
0	1	1	1	AIN 7
1	x	x	x	None

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23.4.2.4. Comparator Output Filter Selection Register (CPTFLS)

Address: COMP0_BASEADDR+0x0000_0000, COMP1_BASEADDR+0x0000_0000

	7	6	5	4	3	2	1	0
Read: Write:	CMFLEN	CMFL_WIDTH[6:0]						
Reset:	0	0	0	0	0	0	0	0

Figure 23-5: Comparator Output Filter Selection Register(CPTFLS)

CMFLEN — Comparator Output Digital Filter Enable

1 = Comparator Output digital filter is enabled, and CPMRIF and CPMFIF are generated by filter output;

0 = Comparator Output digital filter is disabled, and CPMRIF and CPMFIF are generated by raw output;

CMFL_WIDTH[6:0] — Comparator Output Digital Filter Pulse Width Selection.

CMFL_WIDTH[6:0] determine the width of the input pulse that will be filtered. If the input pulse width is less than (CMFL_WIDTH[6:0]+2) * Period of fips, the pulse will be filtered.

23.5. Function Description

The Comparator inputs are selected in the CPTMX register. The CMXP3–CMXP0 bits select the Comparator positive input; the CMXN3–CMXN0 bits select the Comparator negative input. **Important Note About Comparator Inputs:** The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register and the input, output, pullup and pulldown control should be disabled.

The Comparator output can be polled in software, used as an interrupt source, and/or routed to a Port pin. When routed to a Port pin, the Comparator output is available and asynchronous or synchronous to the system clock; the asynchronous output is available even in STOP mode (with no active system clock). When disabled, the Comparator output defaults to the logic low state, and its supply current falls to less than 100nA.

The Comparator hysteresis is software-programmable via its Comparator Control register CPTCN. Users can program the value of the hysteresis voltage. The Comparator hysteresis is programmed using Bits1–0 in the Comparator Control Register CPTCN.

Comparator interrupts can be generated on both rising-edge and falling-edge output transitions. The CPFIF flag is set to logic 1 upon a Comparator falling-edge occurrence, and the CPRIF flag is set to logic 1 upon the Comparator rising-edge occurrence. Once set, these bits remain set until cleared by software. The Comparator rising-edge interrupt mask is enabled by setting CPRIE to a logic 1. The Comparator falling-edge interrupt mask is enabled by setting CPFIE to a logic 1.

The output state of the Comparator can be obtained at any time by reading the CPOUT bit. The Comparator is enabled by setting the CPEN bit to logic 1, and is disabled by clearing this bit to logic 0.

Note that false rising edges and falling edges can be detected when the comparator is first powered on or if changes are made to the hysteresis control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed. The least start-up time of the comparator is less than 5us.

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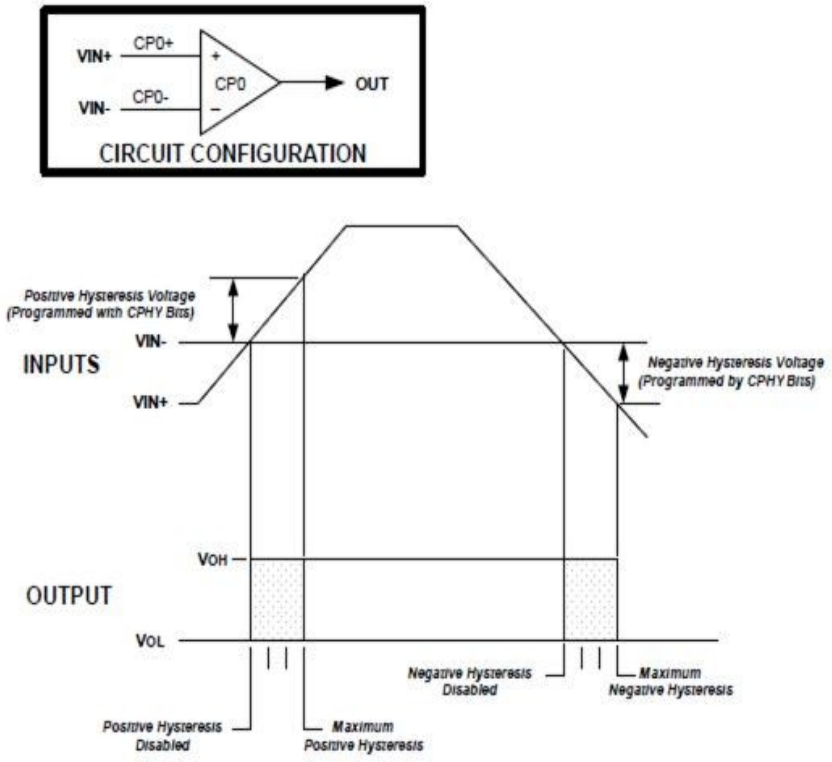


Figure 23-6: Comparator Hysteresis Plot

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24. USB2.0 Full-Speed Device Controller (USBC)

24.1. Introduction

This section describes the USB2.0 Full Speed Device-Only controller. The device implementation in this module provides solutions for implementing a USB 2.0 full-speed/low-speed compliant peripheral.

24.2. Features

Features of the USB module include:

- USB2.0 Device-Only Function Controller
- USB 2.0 Compliant
  – 12 Mbps Full-Speed (FS) Data Rate
  – USB Data Control Logic:
    Packet identification and decoding/generation
    CRC generation and checking
    NRZI (non-return-to-zero inverted) encoding/decoding
    Bit-stuffing
    Sync detection
    End-of-packet detection
- Eight USB Endpoints
- USB RAM
  – 2048 bytes of buffer RAM shared between system and USB module
  – RAM may be allocated as buffers for USB controller or extra system RAM resource
- USB Reset Options
  – USB Module reset generated by MCU
  – Bus reset generated by the host, which triggers a CPU interrupt
- Suspend and Resume Operations with Remote Wakeup Support
- Transceiver Features
  – Converts USB differential voltages to digital logic signal levels
  – On-chip USB Pullup Resistor
- On-chip 3.3 -V Regulator

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24.3. Block Diagram

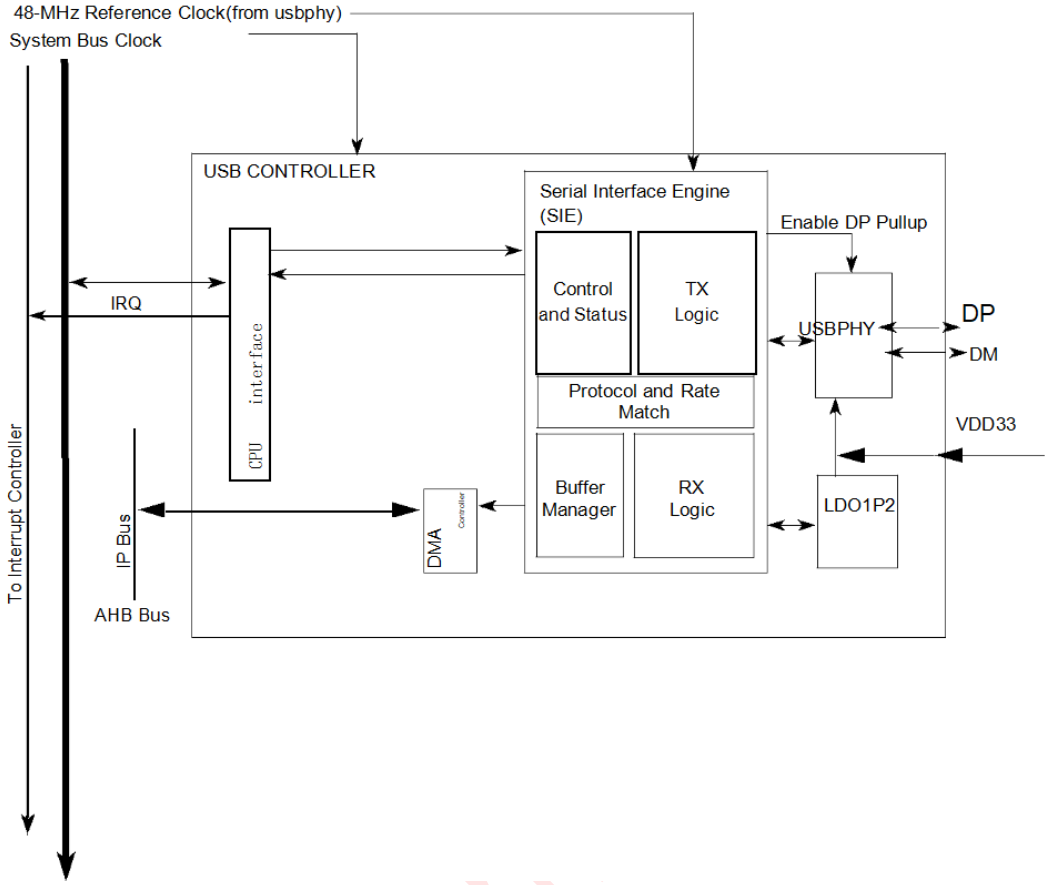


Figure 24-1: USB Full-speed Device(USB module) Block Diagram

24.4. Modes Of Operation

This subsection describes the three low-power modes.

24.4.1. Wait Mode

In wait mode, the USB module can continue to operate normally and can be configured to exit the low-power mode by generating an interrupt request.

24.4.2. Doze Mode

In Doze mode, the USB module can continue to operate normally and can be configured to exit the low-power mode by generating an interrupt request.

24.4.3. Stop Mode

The USB Module is optionally available in stop mode. A reduced current consumption mode may be required for USB suspend mode per USB Specification Rev. 2.0, and stop mode is useful for achieving lower current consumption for the MCU and hence the overall USB device. Before entering stop via firmware, users must ensure that the device settings are configured for stop such that the USB suspend current consumption targets are achieved .

The USB module is notified about entering suspend mode when the SLEEP flag is set; this occurs after the USB bus is idle for 3ms. The USB device suspend mode current consumption level requirements are defined by the USB Specification Rev. 2.0 (500uA for low-power and 2.5mA for high-power with remote-wakeup

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enabled).

If USBRESMEN is set, and a K-state (resume signaling) is detected on the USB bus, the RESUME bit will become set. This will trigger an asynchronous interrupt that will wake the MCU from stop mode and enable clocks to the USB module.

24.5. Memory Map and Registers

The USB Module memory map is shown in **Table 24-1**. The USB Controller base address is 0x4016_0000. This subsection describes the memory map and register structure for USB module.

24.5.1. Memory Map

Refer to **Table 24-1** for a description of the memory map.

Table 24-1: USB Module Memory Map

Offset Address	Bits[31:0]	Access(1)
0x0000	Reserved	S/U
0x0004	Reserved	S/U
0x0008	Reserved	S/U
0x000C	Reserved	S/U
0x001C	USBPHY Control Register 1 (USBPHY_CTRL1)	S/U
0x0080	Interrupt Status Register (INT_STAT)	S/U
0x0084	Interrupt Enable Register (INT_ENB)	S/U
0x0088	Error Interrupt Status Register (ERR_STAT)	S/U
0x008C	Error Interrupt Enable Register (ERR_ENB)	S/U
0x0090	Status Register (STAT)	S/U
0x0094	Control Register (CTL)	S/U
0x0098	Address Register (ADDR)	S/U
0x009C	EBT Page Register 1 (EBT_PAGE_01)	S/U
0x00A0	Frame Number Register (FRMNUML)	S/U
0x00A4	Frame Number Register (FRMNUMH)	S/U
0x00A8	Token Register (TOKEN)	S/U
0x00AC	SOF Threshold Register (SOF_THLD)	S/U
0x00B0	EBT Page Register 2 (EBT_PAGE_02)	S/U
0x00B4	EBT Page Register 3 (EBT_PAGE_03)	S/U
0x00C0	Endpoint Control Registers (ENDPT0)	S/U
0x00C4	Endpoint Control Registers (ENDPT1)	S/U
0x00C8	Endpoint Control Registers (ENDPT2)	S/U
0x00CC	Endpoint Control Registers (ENDPT3)	S/U
0x00D0	Endpoint Control Registers (ENDPT4)	S/U
0x00D4	Endpoint Control Registers (ENDPT5)	S/U
0x00D8	Endpoint Control Registers (ENDPT6)	S/U

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Offset Address	Bits[31:0]	Access(1)
0x00DC	Endpoint Control Registers (ENDPT7)	S/U
0x0100	USBPHY Control Register 2 (USBPHY_CTRL2)	S/U
0x0104	USB PHY Observe Register (USB_PHY_OBSERVE)	S/U
0x0108	USB PHY GPIO Register	S/U
0x010C	USB Resume Wakeup Enable Register (USB_RESMEN)	S/U
0x0118	USBPHY Control Register 3 (USBPHY_CTRL3)	S/U
0x011C	USBPHY Control Register 4 (USBPHY_CTRL4)	S/U

Note (1) : S = CPU supervisor mode access only. S/U = CPU supervisor or user mode access. Accessing supervisor only address in user mode has no effect and result in a cycle termination transfer error.

24.5.2. Register Descriptions

24.5.2.1. USBPHY Control Register 1 (USBPHY_CTRL1)

The USBPHY Control Register controls the operation of Data Line termination resistors.

Address: USBC_BASEADDR+0x0000_001C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	DP_HIGH	0						
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-2: USBPHY Control Register 1 (USBPHY_CTRL1)

DP_HIGH — D+ Data Line pullup resistor enable

0 = D+ pullup resistor is disabled

1 = D+ pullup resistor is enabled.

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24.5.2.2. Interrupt Status Register (INT_STAT)

The Interrupt Status Register contains bits for each of the interrupt sources within the USB Module. Each of these bits is qualified with their respective interrupt enable bits. All bits of this register are logically OR'd together along with the OTG Interrupt Status Register (OTG_STAT) to form a single interrupt source for the processor's interrupt controller. After an interrupt bit has been set it may only be cleared by writing a one to the respective interrupt bit. This register contains the value of 0x00 after a reset.

Address: USBC_BASEADDR+0x0000_0080

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	STALL	0	RESUME	SLEEP	TOKDNE	SOF_TOK	ERROR	USB_RST
Write:								
Reset:	0	0	0	1	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-3: Interrupt Status Register (INT_STAT)

STALL — Stall Interrupt, and cleared by writing 1 to this bit.

In Device mode this bit is asserted when a STALL handshake is sent by the USB Module. In Host mode this bit is set when the USB Module detects a STALL acknowledge during the handshake phase of a USB transaction. This interrupt can be used to determine whether the last USB transaction was completed successfully or if it stalled.

RESUME — Resume Interrupt, and cleared by writing 1 to this bit.

This bit is set depending on the DP/DM signals, and can be used to signal remote wake-up signaling on the USB bus. When not in suspend mode, this interrupt should be disabled.

SLEEP — Sleep Interrupt, and cleared by writing 1 to this bit.

This bit is set when the USB Module detects a constant idle on the USB bus for 3 milliseconds. The sleep timer is reset by activity on the USB bus.

TOKDNE — Token Done Interrupt, and cleared by writing 1 to this bit.

This bit is set when the current token being processed has completed. The processor should immediately read the STAT register to determine the EndPoint and EB entry used for this token. Clearing this bit (by writing a one) causes the STAT register to be cleared or the STAT holding register to be loaded into the STAT register.

SOF_TOK — SOF Token Interrupt, and cleared by writing 1 to this bit.

This bit is set when the USB Module receives a Start Of Frame (SOF) token. In Host mode this bit is set when the SOF threshold is reached, so that software can prepare for the next SOF.

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ERROR — Error Interrupt, and cleared by writing 1 to this bit.

This bit is set when any of the error conditions within the ERR_STAT register occurs. The processor must then read the ERR_STAT register to determine the source of the error.

USB_RST — USB RST Interrupt, and cleared by writing 1 to this bit.

This bit is set when the USB Module has decoded a valid USB reset. This informs the Microprocessor that it should write 0x00 into the address register and enable endpoint 0. USB_RST is set after a USB reset has been detected for 2.5 microseconds. It is not asserted again until the USB reset condition has been removed and then reasserted.

24.5.2.3. Interrupt Enable Register (INT_ENB)

The Interrupt Enable Register contains enable bits for each of the interrupt sources within the USB Module. Setting any of these bits enables the respective interrupt source in the INT_STAT register. This register contains the value of 0x00 after a reset.

Address: USBC_BASEADDR+0x0000_0084

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	STALL_EN	ATTACH_EN	RESUME_EN	SLEEP_EN	TOKDNE_EN	SOF_TOK_EN	ERROR_EN	USB_RST_EN
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-4: Interrupt Enable Register (INT_ENB)

STALL_EN — Stall Interrupt Enable

0 = Stall Interrupt is disabled

1 = Stall Interrupt is enabled.

ATTACH_EN — Attach Interrupt Enable.

0 = Attach Interrupt is disabled.

1 = Attach Interrupt is enabled.

RESUME_EN — Resume Interrupt Enable.

0 = Resume Interrupt is disabled.

1 = Resume Interrupt is enabled.

SLEEP_EN — Sleep Interrupt Enable.

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0 = Sleep Interrupt is disabled.
1 = Sleep Interrupt is enabled.

TOKDNE_EN — Token Done Interrupt Enable.
0 = Token Done Interrupt is disabled.
1 = Token Done Interrupt is enabled.

SOF_TOK_EN — SOF Toke Interrupt Enable.
0 = SOF Token Interrupt is disabled.
1 = SOF Token Interrupt is enabled.

ERROR_EN — Error Interrupt Enable.
0 = Error Interrupt is disabled.
1 = Error Interrupt is enabled.

USB_RST_EN — USB Reset Interrupt Enable.
0 = USB Reset Interrupt is disabled.
1 = USB Reset Interrupt is enabled.

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24.5.2.4. Error Interrupt Status Register (ERR_STAT)

The Error Interrupt Status Register contains enable bits for each of the error sources within the USB Module. Each of these bits is qualified with their respective error enable bits. All bits of this Register are logically OR'd together and the result is placed in the ERROR bit of the INT_STAT register. After an interrupt bit has been set it may only be cleared by writing a one to the respective interrupt bit. Each bit is set as soon as the error conditions is detected. Therefore, the interrupt does not typically correspond with the end of a token being processed. This register contains the value of 0x00 after a reset.

Address: USBC_BASEADDR+0x0000_0088

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	BTS_ERR	0	DMA_ERR	BTO_ERR	DFN8	CRC16	CRC5_EOF	PID_ERR
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-5: Error Interrupt Status Register (ERR_STAT)

BTS_ERR — This bit is set when a bit stuff error is detected. If set, the corresponding packet is rejected due to the error.

DMA_ERR — This bit is set if the USB Module has requested a DMA access to read a new EBT but has not been given the bus before it needs to receive or transmit data. If processing a TX transfer, this would cause a transmit data underflow condition. If processing a RX transfer, this would cause a receive data overflow condition. This interrupt is useful when developing device arbitration hardware for the microprocessor and the USB Module to minimize bus request and bus grant latency. This bit is also set if a data packet to or from the host is larger than the buffer size allocated in the EBT. In this case the data packet is truncated as it is put into buffer memory.

BTO_ERR — This bit is set when a bus turnaround timeout error occurs. The USB Module contains a bus turnaround timer that keeps track of the amount of time elapsed between the token and data phases of a SETUP or OUT TOKEN or the data and handshake phases of a IN TOKEN. If more than 16-bits times are counted from the previous EOP before a transition from IDLE, a bus turnaround timeout error occurs.

DFN8 — This bit is set if the data field received was not 8-bits in length. USB Specification 1.0 requires that data fields be an integral number of bytes. If the data field was not an integral number of bytes, this bit is set.

CRC16 — This bit is set when a data packet is rejected due to a CRC16 error.

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CRC5_EOF — This error interrupt has two functions. When the USB Module is operating in device mode (HOST_MODE_EN = 0), this interrupt detects CRC5 errors in the token packets generated by the host. If set, the token packet was rejected due to a CRC5 error. When the USB Module is operating in host mode (HOST_MODE_EN = 1), this interrupt detects End Of Frame (EOF) error conditions. This occurs when the USB Module is transmitting or receiving data and the SOF counter reaches zero. This interrupt is useful when developing USB packet scheduling software to ensure that no USB transactions cross the start of the next frame.

PID_ERR — This bit is set when the PID check field fails.

24.5.2.5. Error Interrupt Enable Register (ERR_ENB)

The Error Interrupt Enable Register contains enable bits for each of the error interrupt sources within the USB Module. Setting any of these bits enables the respective interrupt source in the ERR_STAT register. Each bit is set as soon as the error conditions is detected. Therefore, the interrupt does not typically correspond with the end of a token being processed. This register contains the value of 0x00 after a reset.

Address: USBC_BASEADDR+0x0000_008C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	BTS_ERR_EN	0	DMA_ERR_EN	BTO_ERR_EN	DFN8_EN	CRC16_EN	CRC5_EOF_EN	PID_ERR_EN
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-6: Error Interrupt Enable Register (ERR_ENB)

BTS_ERR_EN — BTS_ERR Interrupt Enable

0 = BTS_ERR Interrupt is disabled.

1 = BTS_ERR Interrupt is enabled.

DMA_ERR_EN — DMA_ERR Interrupt Enable.

0 = DMA_ERR Interrupt is disabled.

1 = DMA_ERR Interrupt is enabled.

BTO_ERR_EN — BTO_ERR Interrupt Enable.

0 = BTO_ERR Interrupt is disabled.

1 = BTO_ERR Interrupt is enabled.

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DFN8_EN — DFN8 Interrupt Enable.

0 = DFN8 Interrupt is disabled.

1 = DFN8 Interrupt is enabled.

CRC16_EN — CRC16 Interrupt Enable.

0 = CRC16 Interrupt is disabled.

1 = CRC16 Interrupt is enabled.

CRC5_EOF_EN — CRC5_EOF Interrupt Enable.

0 = CRC5_EOF Interrupt is disabled.

1 = CRC5_EOF Interrupt is enabled.

PID_ERR_EN — PID_ERR Interrupt Enable.

0 = PID_ERR Interrupt is disabled.

1 = PID_ERR Interrupt is enabled.

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24.5.2.6. Status Register (STAT)

The Status Register reports the transaction status within the USB Module. When the processor's interrupt controller has received a TOK_DNE interrupt, the Status Register should be read to determine the status of the previous endpoint communication. The data in the status register is valid when the TOK_DNE interrupt bit is asserted. The STAT register is actually a read window into a status FIFO maintained by the USB Module. When the USB Module uses a EB entry, it updates the Status Register. If another USB transaction is performed before the TOK_DNE interrupt is serviced, the USB Module stores the status of the next transaction in the STAT FIFO. Thus the STAT register is actually a four byte FIFO that allows the processor core to process one transaction while the SIE is processing the next transaction. Clearing the TOK_DNE bit in the INT_STAT register causes the SIE to update the STAT register with the contents of the next STAT value. If the data in the STAT holding register is valid, the SIE immediately reasserts to TOK_DNE interrupt.

Address: USBC_BASEADDR+0x0000_0090

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	ENDP[3:0]				TX	ODD	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-7: Status Register (STAT)

ENDP[3:0] — Endpoint Number.

These four bits encode the endpoint address that received or transmitted the previous token. This allows the microcontroller to determine which EBT entry was updated by the last USB transaction.

0000 Endpoint 0
0001 Endpoint 1
0010 Endpoint 2
0011 Endpoint 3
0100 Endpoint 4
0101 Endpoint 5
0110 Endpoint 6
0111 Endpoint 7

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TX — Transmit Indicator.

0 = The most recent transaction was a Receive operation.

1 = The most recent transaction was a Transmit operation.

ODD — Odd/Even Transaction.

This bit is set if the last Endpoint Buffer Table updated was in the odd bank of the EBT.

24.5.2.7. Control Register (CTL)

The Control Register provides various control and configuration information for the USB Module.

Address: USBC_BASEADDR+0x0000_0094

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	JSTATE	SE0	TXSUSPEND/TOKENBUSY	RESET	HOST_MODE_EN	RESUME	ODD_RST	USB_EN/SOF_EN
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-8: Control Register (CTL)

JSTATE — Live USB differential receiver JSTATE signal

The polarity of this signal is affected by the current state of LS_EN .

SE0 — Live USB Single Ended Zero signal

The polarity of this signal is affected by the current state of LS_EN .

TXSUSPEND / TOKENBUSY

When the USB Module is in Host mode, TOKEN_BUSY is set when the USB Module is busy executing a USB token and no more token commands should be written to the Token Register. Software should check this bit before writing any tokens to the Token Register to ensure that token commands are not lost. In Device mode TXSUSPEND is set when the SIE has disabled packet transmission and reception. Clearing this bit allows the SIE to continue token processing. This bit is set by the SIE when a Setup Token is received, allowing software to dequeue any pending packet transactions in the EBT before resuming token processing.

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RESET — This bit is invalid for current device-role-only function.

Setting this bit enables the USB Module to generate USB reset signaling. This allows the USB Module to reset USB peripherals. This control signal is only valid in Host mode (HOST_MODE_EN = 1). Software must set RESET to 1 for the required amount of time and then clear it to 0 to end reset signaling.

HOST_MODE_EN — This bit is read-only for this device-role-only function.

When set to 1, this bit enables the USB Module to operate in Host mode. In host mode, the USB module performs USB transactions under the programmed control of the host processor.

RESUME

When set to 1, this bit enables the USB Module to execute resume signaling.

This allows the USB Module to perform remote wake-up. Software must set RESUME to 1 for the required amount of time and then clear it to 0. If the HOST_MODE_EN bit is set, the USB module appends a Low Speed End of Packet to the Resume signaling when the RESUME bit is cleared.

ODD_RST

Setting this bit to 1 resets all the EBT ODD ping/pong bits to 0, which then specifies the EVEN EBT bank.

USB_EN/SOF_EN — USB Enable.

Setting this bit causes the SIE to reset all of its ODD bits to the EBTs. Therefore, setting this bit resets much of the logic in the SIE. When host mode is enabled, clearing this bit causes the SIE to stop sending SOF tokens.

0 = The USB Module is disabled.

1 = The USB Module is enabled.

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24.5.2.8. Address Register (ADDR)

The Address Register holds the unique USB address that the USB Module decodes when in Peripheral mode (HOST_MODE_EN = 0). When operating in Host mode (HOST_MODE_EN = 1) the USB Module transmits this address with a TOKEN packet. This enables the USB Module to uniquely address an USB peripheral. In either mode, the USB_EN bit within the control register must be set. The Address Register is reset to 0x00 after the reset input becomes active or the USB Module decodes a USB reset signal. This action initializes the Address Register to decode address 0x00 as required by the USB specification.

Address: USBC_BASEADDR+0x0000_0098

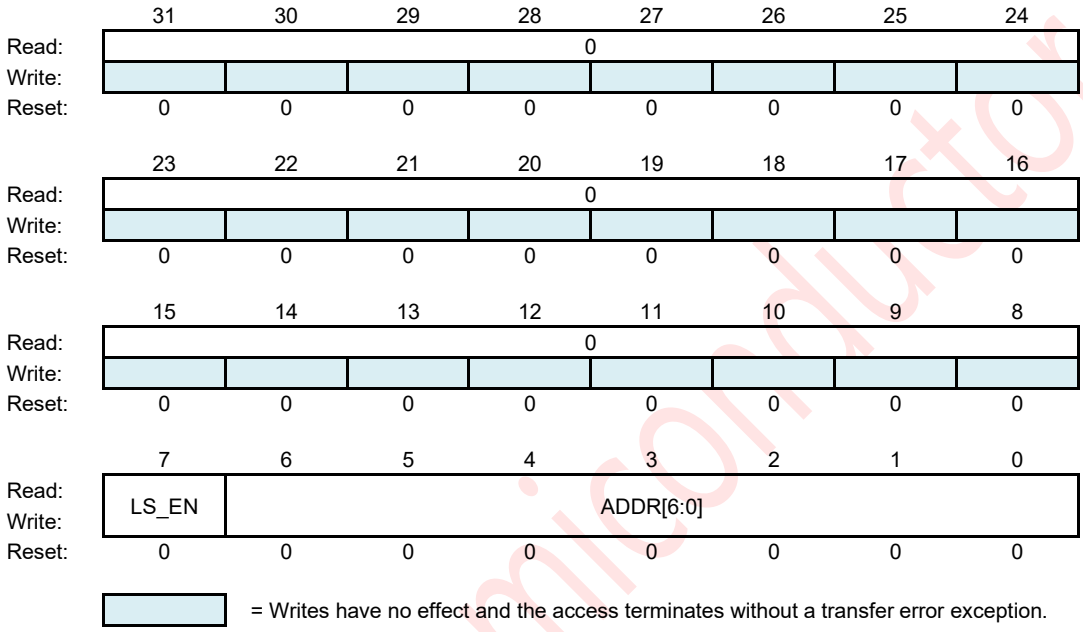


Figure 24-9: Address Register (ADDR)

LS_EN — Low Speed Enable bit.

This bit informs the USB Module that the next token command written to the token register must be performed at low speed. This enables the USB Module to perform the necessary preamble required for low-speed data transmissions.

ADDR[6:0] — USB address.

This 7-bits value defines the USB address that the USB Module decodes in peripheral mode, or transmits when in host mode.

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24.5.2.9. EBT Page Register 1 (EBT_PAGE_01)

Address: USBC_BASEADDR+0x0000_009C

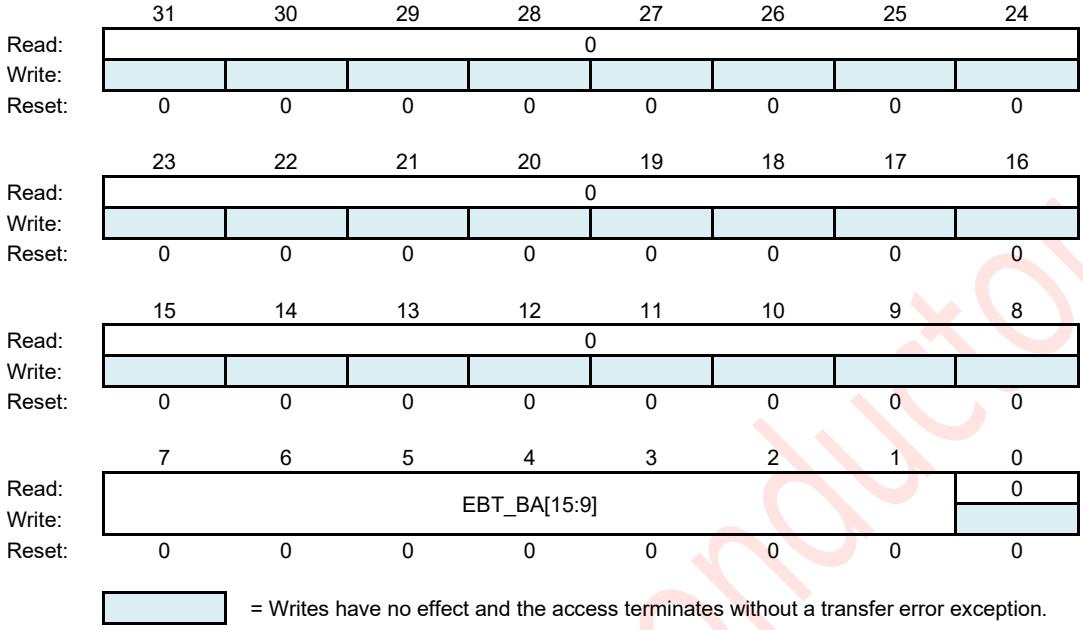


Figure 24-10: EBT Page Register 1 (EBT_PAGE_01)

EBT_BA[15:9] — This 7-bits field provides address bits 15 through 9 of the EBT base address, which defines where the Buffer Descriptor Table resides in system memory.

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24.5.2.10. Frame Number Register (FRMNUML)

The Frame Number Registers contains the 11-bits frame number. The Frame Number Register requires two 8-bits registers to implement. The low order byte is contained in FRMNUML, and the high order byte is contained in FRMNUMH. These registers are updated with the current frame number whenever a SOF TOKEN is received.

Address: USBC_BASEADDR+0x0000_00A0

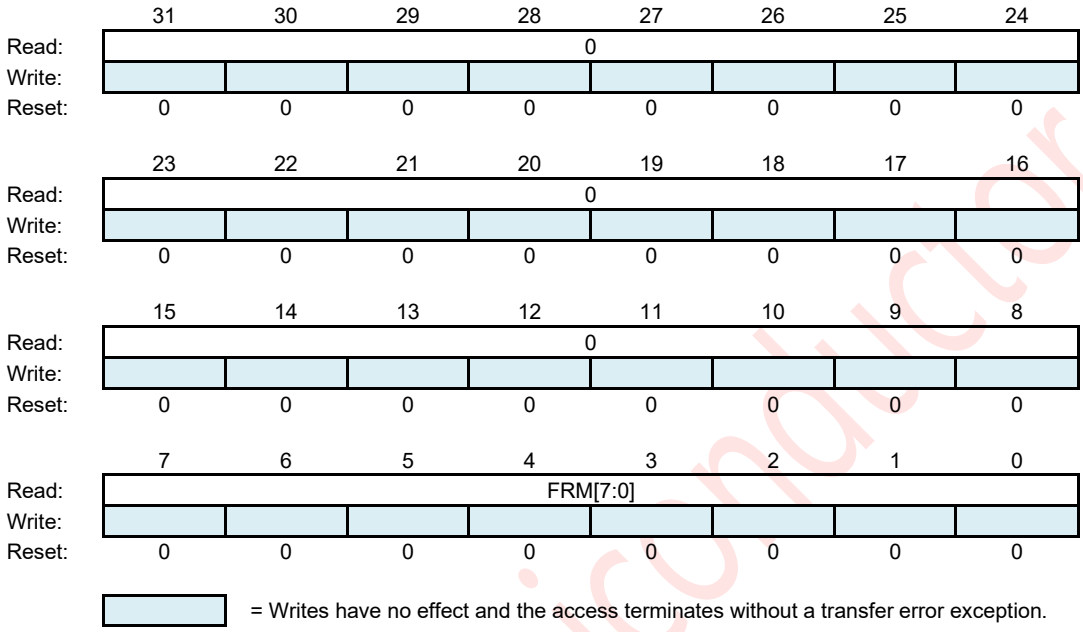


Figure 24-11: Frame Number Register (FRMNUML)

FRM[7:0] — Frame Number.

These bits represent the low order bits of the 11 bit Frame Number.

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24.5.2.11. Frame Number Register (FRMNUMH)

The Frame Number Registers contains the 11-bits frame number. The Frame Number Register requires two 8-bits registers to implement. The low order byte is contained in FRMNUML, and the high order byte is contained in FRMNUMH. These registers are updated with the current frame number whenever a SOF TOKEN is received.

Address: USBC_BASEADDR+0x0000_00A4

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:						FRM[10:8]		
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-12: Frame Number Register (FRMNUMH)

FRM[10:8] — Frame Number.

These bits represent the high order bits of the 11-bits Frame Number.

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24.5.2.12. Token Register (TOKEN)

The Token Register is used to perform USB transactions when in host mode (HOST_MODE_EN = 1). When the processor core wishes to execute a USB transaction to a peripheral, it writes the TOKEN type and endpoint to this register. After this register has been written, the USB module begins the specified USB transaction to the address contained in the address register. The processor core should always check that the TOKEN_BUSY bit in the control register is not set before performing a write to the Token Register. This ensures token commands are not overwritten before they can be executed. The address register and endpoint control register 0 are also used when performing a token command and therefore must also be written before the Token Register. The address register is used to correctly select the USB peripheral address transmitted by the token command. The endpoint control register determines the handshake and retry policies used during the transfer.

Address: USBC_BASEADDR+0x0000_00A8

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	TOKEN_PID[3:0]				TOKEN_ENDPT[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-13: Token Register (TOKEN)

TOKEN_PID[3:0] — This 4-bits field contains the token type executed by the USB Module.

0001 OUT Token. USB Module performs an OUT (TX) transaction.
1001 IN Token. USB Module performs an In (RX) transaction.
1101 SETUP Token. USB Module performs a SETUP (TX) transaction

TOKEN_ENDPT[3:0] — This 4-bits field holds the Endpoint address for the token command. The 4-bits value written must be a valid endpoint.

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24.5.2.13. SOF Threshold Register (SOF_THLD)

The SOF Threshold Register is used only in Host mode (HOST_MODE_EN = 1). When in Host mode, the 14-bits SOF counter counts the interval between SOF frames. The SOF must be transmitted every 1msec so the SOF counter is loaded with a value of 12000. When the SOF counter reaches zero, a Start Of Frame (SOF) token is transmitted. The SOF threshold register is used to program the number of USB byte times before the SOF to stop initiating token packet transactions. This register must be set to a value that ensures that other packets are not actively being transmitted when the SOF time counts to zero. When the SOF counter reaches the threshold value, no more tokens are transmitted until after the SOF has been transmitted. The value programmed into the threshold register must reserve enough time to ensure the worst case transaction completes. In general, the worst case transaction is a IN token followed by a data packet from the target followed by the response from the host. The actual time required is a function of the maximum packet size on the bus. Typical values for the SOF threshold are:

64-byte packets = 74;

32-byte packets = 42;

16-byte packets = 26;

8-byte packets = 18.

Address: USBC_BASEADDR+0x0000_00AC

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	CNT[7:0]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-14: SOF Threshold Register (SOF_THLD)

CNT[7:0] — This 8-bits field represents the SOF count threshold in byte times. This register is read only in this device.

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24.5.2.14. EBT Page Register 2 (EBT_PAGE_02)

The Endpoint Buffer Table Page Register 2 contains an 8-bits value used to compute the address where the current Endpoint Buffer Table (EBT) resides in system memory.

Address: USBC_BASEADDR+0x0000_00B0

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	EBT_BA[23:16]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-15: EBT Page Register 2 (EBT_PAGE_02)

EBT_BA[23:16]

This 8-bits field provides address bits 23 through 16 of the EBT base address, which defines where the Buffer Descriptor Table resides in system memory.

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24.5.2.15. EBT Page Register 3 (EBT_PAGE_03)

The Endpoint Buffer Table Page Register 3 contains an 8-bits value used to compute the address where the current Endpoint Buffer Table (EBT) resides in system memory.

Address: USBC_BASEADDR+0x0000_00B4

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	EBT_BA[31:24]							
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-16: EBT Page Register 3 (EBT_PAGE_03)

EBT_BA[31:24]

This 8-bits field provides address bits 31 through 24 of the EBT base address, which defines where the Buffer Descriptor Table resides in system memory.

24.5.2.16. Endpoint Control Registers (ENDPTn)

The Endpoint Control Registers contain the endpoint control bits for each of the 8 endpoints available within the USB Module for a decoded address. The format for these registers is shown in the following figure. Endpoint 0 (ENDPT0) is associated with control pipe 0, which is required for all USB functions. Therefore, after a USB_RST interrupt occurs, the processor core should set the ENDPT0 register to contain 0x0D.

In Host mode, ENDPT0 is used to determine the handshake, retry and low speed characteristics of the host transfer. For Host mode control, bulk, and interrupt transfers the EP_HSHK bit should be set to 1. For Isochronous transfers, it should be set to 0. Common values to use for ENDPT0 in host mode are 0x4D for Control, Bulk, and Interrupt transfers, and 0x4C for Isochronous transfers.

Registers Offset address:

ENDPT0 Address: USBC_BASEADDR+0x0000_00C0
ENDPT1 Address: USBC_BASEADDR+0x0000_00C4
ENDPT2 Address: USBC_BASEADDR+0x0000_00C8
ENDPT3 Address: USBC_BASEADDR+0x0000_00CC
ENDPT4 Address: USBC_BASEADDR+0x0000_00D0
ENDPT5 Address: USBC_BASEADDR+0x0000_00D4
ENDPT6 Address: USBC_BASEADDR+0x0000_00D8
ENDPT7 Address: USBC_BASEADDR+0x0000_00DC

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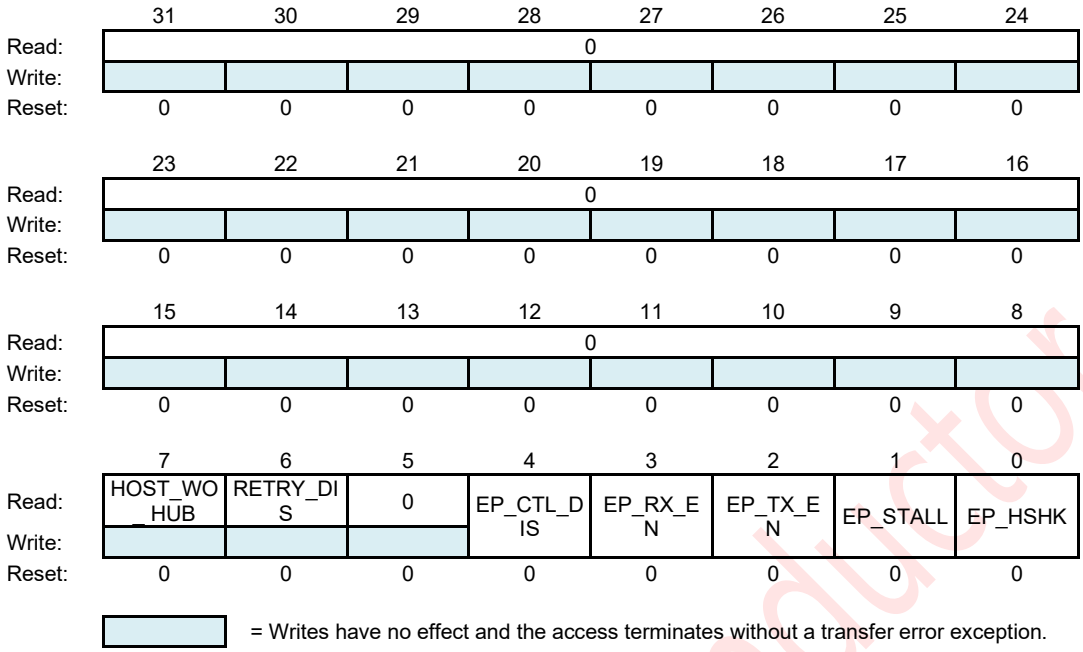


Figure 24-17: Endpoint Control Registers(ENDPTn, n = 0-7)

HOST_WO_HUB — This is a Host mode only bit and is only present in the control register for endpoint 0 (ENDPT0). This bit is read only in this device.

When set, this bit allows the host to communicate to a directly connected low speed device. When cleared, the host produces the PRE_PID, then switches to low speed signaling, when sending a token to a low speed device as required to communicate with a low speed device through a hub.

RETRY_DIS — This is a Host mode only bit and is only present in the control register for endpoint 0 (ENDPT0). This bit is read only in this device.

When set, this bit causes the host to not retry NAK'ed (Negative Acknowledgement) transactions. When a transaction is NAKed, the EBT PID field is updated with the NAK PID, and the TOKEN_DNE interrupt is set. When this bit is cleared, NAKed transactions is retried in hardware. This bit must be set when the host is attempting to poll an interrupt endpoint.

EP_CTL_DIS — This bit, when set, disables control (SETUP) transfers. When this bit is cleared, control transfers are enabled. This applies if and only if the EP_RX_EN and EP_TX_EN bits are also set.

EP_RX_EN — This bit, when set, enables the endpoint for RX transfers.

EP_TX_EN — This bit, when set, enables the endpoint for TX transfers.

EP_STALL — When set, this bit indicates that the endpoint is stalled. This bit has priority over all other control bits in the EndPoint Enable Register, but it is only valid if EP_TX_EN = 1 or EP_RX_EN = 1. Any access to this endpoint causes the USB Module to return a STALL handshake. After an endpoint is stalled, it requires intervention from the Host Controller.

EP_HSHK — When set, this bit enables an endpoint to perform handshaking during a transaction to this endpoint. This bit is generally set unless the endpoint is Isochronous.

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Table 24-2: Endpoint Enable/Direction Control

Bit Name			Endpoint Enable/Direction Control
EP_CTL_DIS	EP_RX_EN	EP_TX_EN	
X	0	0	Disable endpoint
X	0	1	Enable endpoint for IN(TX) transfers only
X	1	0	Enable endpoint for OUT(RX) transfers only
0	1	1	Enable endpoint for IN, OUT and SETUP transfers.
1	1	1	RESERVE

24.5.2.17. USBPHY Control Register 2 (USBPHY_CTRL2)

Address: USBC_BASEADDR+0x0000_0100

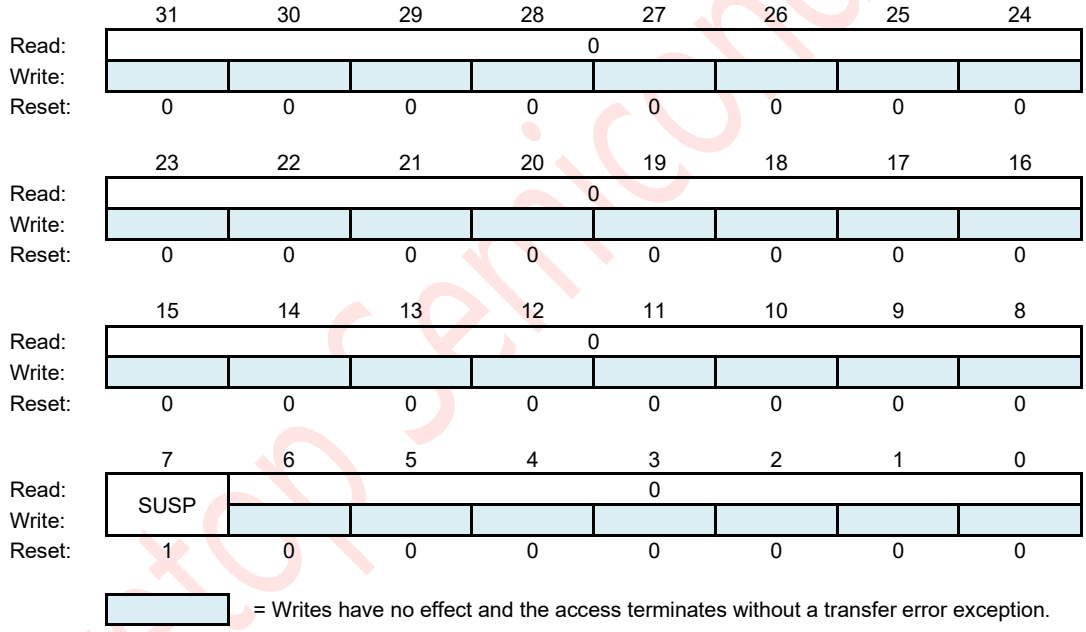


Figure 24-18: USBPHY Control Register 2 (USBPHY_CTRL2)

SUSP — Places the USB transceiver into the suspend state.

0 = USB transceiver is not in suspend state.

1 = USB transceiver is in suspend state.

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24.5.2.18. USB PHY Observe Register (USB_PHY_OBSERVE)

Address: USBC_BASEADDR+0x0000_0104

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	DP_PU	0						
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-19: USB PHY Observe Register (USB_PHY_OBSERVE)

DP_PU — Provides observability of the D+ Pull Up signal output from the USB OTG module. This bit is useful when interfacing to an external OTG control module via a serial interface.

0 = D+ pullup is disabled.

1 = D+ pullup is enabled.

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24.5.2.19. USBPHY GPIO Register (USB_PHY_GPIO)

Address: USBC_BASEADDR+0x0000_0108

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	GPIOEN	RX_RCV	RX_DM	RX_DP	TX_DM_EN	TX_DP_EN	TX_DM	TX_DP
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-20: USB PHY GPIO Register (USB_PHY_GPIO)

GPIOEN — USB PHY GPIO Mode control.
0 = USB PHY is not in GPIO Mode
1 = USB PHY is in GPIO Mode

RX_RCV — USB PHY Differential input data during USBPHY GPIO mode.

RX_DM — USB PHY DM input data during USBPHY GPIO mode.

RX_DP — USB PHY DP input data during USBPHY GPIO mode.

TX_DM_EN — USB PHY DM output direction control during USBPHY GPIO mode.
0 = DM is input direction
1 = DM is output direction

TX_DP_EN — USB PHY DP output direction control during USBPHY GPIO mode.
0 = DP is input direction
1 = DP is output direction

TX_DM — USB PHY DM output data during USBPHY GPIO mode.

TX_DP — USB PHY DP output data during USBPHY GPIO mode.

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24.5.2.20. USB Resume Enable Register (USB_RESMEN)

Address: USBC_BASEADDR+0x0000_010C

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0	0	USBRESMEN	USBPHYCLKEN	0	0	USBIRQ	RESUME
Write:	USB_SFT_RESET							
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 24-21: USB Resume Enable Register (USB_RESMEN)

USB_SFT_RESET — USB Soft Reset control bit.

The USB Module will be reset by writing a one to this bit.

USBRESMEN — USB resume wakeup enable control bit

If USBRESMEN is set, and a K-state (resume signaling) is detected on the USB bus, the RESUME bit will become set. This will trigger an asynchronous interrupt that will wake the MCU from stop mode and enable clocks to the USB module.

USBPHYCLKEN — USB PHY clock enable control bit.

USBIRQ — All enabled interrupt in INT_STAT register.

This bit will be set if any one of INT_STAT is set and the corresponding INT_ENB is set.

RESUME — USB DP/DM resume status bit.

If USBRESMEN is set, and a K-state (resume signaling) is detected on the USB bus, this bit will be set when CPU is waked-up from stop mode and cleared by clearing USBRESMEN bit.

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24.5.2.21. USB PHY Control Register3 (USBPHY_CTRL3)

Address: USBC_BASEADDR+0x0000_0118

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read: / Write:	PHY_1.5V PDnote1	PHY_OEN note1	PHY_RESETb	USB_BYTE_SWAP	PLL_PD	PHY_SUSPEND	PHY_SUSPEND_SEL	48_60M_SEL
Reset:	0	0	0	0	1	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

note1 These bits are meaning-less in this chip

Figure 24-22: USB PHY Control Register 3 (USBPHY_CTRL3)

PHY_1.5VPD — USB PHY core power control.

0 = USB PHY core power supply will not be lost.

1 = USB PHY core power supply will be lost.

PHY_OEN — USB PHY output isolate control.

0 = USB PHY output will not be isolated.

1 = USB PHY output will be isolated.

PHY_RESETb — USB PHY RESET control.

0 = USB PHY will be in RESET state.

1 = USB PHY will be NORMAL state.

USB_BYTE_SWAP — When this bit is set, the data received/transmitted by USB will be swapped when reading from or writing to the system memory.

0 = USB Received or Transmit data will not be swapped.

1 = USB Received or Transmit data will be swapped.

PLL_PD — USB PHY PLL power down mode control.

0 = USB PHY PLL is not in power down state.

1 = USB PHY PLL is in power down state.

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PHY_SUSPEND — USB PHY Suspend control

0 = USB PHY is not in Suspend state.

1 = USB PHY is in Suspend state.

PHY_SUSPEND_SEL — USB PHY Suspend control selection.

0 = USB PHY Suspend is controlled by USBPHY_CTRL2[SUSP].

1 = USB PHY Suspend is controlled by USBPHY_CTRL3[PHY_SUSPEND].

48_60M_SEL — USB PHY 48/60Mhz clock selection.

0 = 48Mhz is used as USB SIE decode clock.

1 = 60Mhz is used as USB SIE decode clock.

24.5.2.22. USB PHY Control Register4 (USBPHY_CTRL4)

Address: USBC_BASEADDR+0x0000_011C

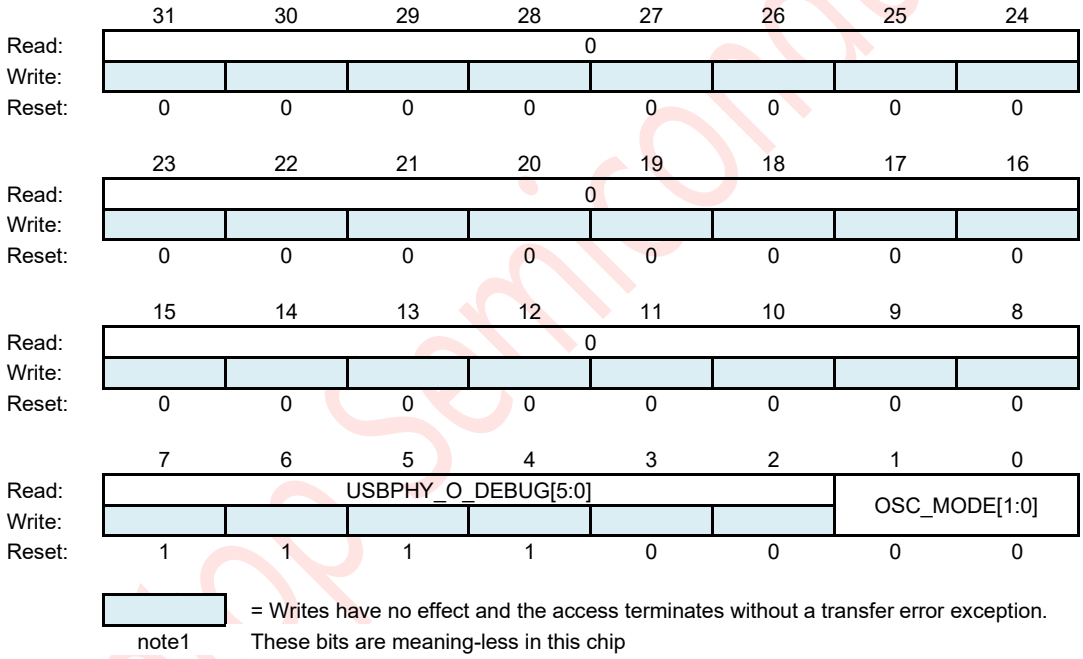


Figure 24-23: USB PHY Control Register 4 (USBPHY_CTRL4)

USBPHY_O_DEBUG[5:0] — USBPHY Output signals are for debug purpose and are meaningless during normal work.

OSC_MODE[1:0] — USB PHY clock mode selection.

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Table 24-3: USB PHY Oscillator Mode Selection

OSC_MODE[1:0]	Oscillator Mode Selection
00	Auto detection oscillator
01	Auto detection oscillator (fast simulation mode)
10	Selection internal oscillator
11	Selection external oscillator

24.6. Function Description

The USB-FS 2.0 full-speed/low-speed module communicates with the processor core through status registers, control registers, and data structures in memory.

24.6.1. Data Structure

The function of the device operation is to transfer a request in the memory image to and from the Universal Serial Bus. To efficiently manage USB endpoint communications, the USB module implements an Endpoint Buffer Table (EBT) in system memory. See **Figure 24-24**.

24.6.2. Endpoint Buffer Table

To efficiently manage USB endpoint communications the USB module implements a Buffer Descriptor Table (EBT) in system memory. The EBT resides on a 512 byte boundary in system memory and is pointed to by the EBT Page Registers. Every endpoint direction requires two eight-byte Endpoint Buffer Table entries.

Therefore, a system with 16 fully bidirectional endpoints would require 512 bytes of system memory to implement the EBT. The two Endpoint Buffer Table (EBT) entries allows for an EVEN EB entry and ODD EB entry for each endpoint direction. This allows the microprocessor to process one EB entry while the USB module is processing the other EB entry. Double buffering EB entrys in this way allows the USB SIE to easily transfer data at the maximum throughput provided by USB.

The software API intelligently manages buffers for the USB SIE by updating the EBT when needed. This allows the USB SIE to efficiently manage data transmission and reception, while the microprocessor performs communication overhead processing and other function dependent applications. Because the buffers are shared between the microprocessor and the USB module, a simple semaphore mechanism is used to distinguish who is allowed to update the EBT and buffers in system memory. A semaphore bit, the OWN bit, is cleared to 0 when the EB entry is owned by the microprocessor. The microprocessor is allowed read and write access to the EB entry and the buffer in system memory when the OWN bit is 0. When the OWN bit is set to 1, the EB entry and the buffer in system memory are owned by the USB module. The USB module now has full read and write access and the microprocessor should not modify the EB entry or its corresponding data buffer. The EB entry also contains indirect address pointers to where the actual buffer resides in system memory. This indirect address mechanism is shown in the following diagram.

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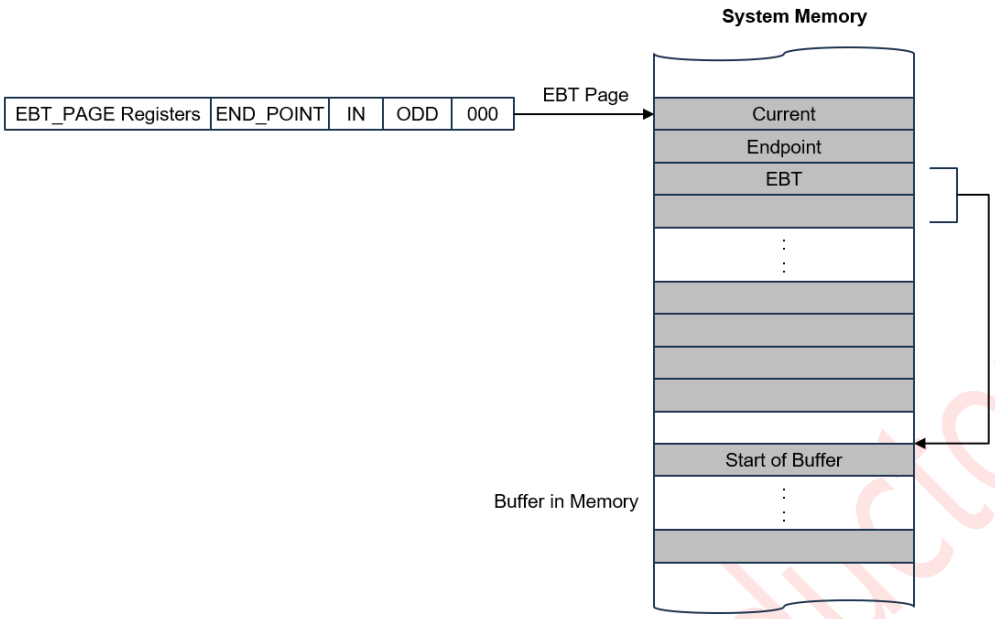


Figure 24-24: Endpoint Buffer Table

24.6.3. Rx vs. Tx As A USB Target Device

The centric nomenclature is used to describe the direction of the data transfer between the USB SIE core and the USB Host:

Rx (or receive): describes transfers that move data from the USB to memory.

Tx (or transmit): describes transfers that move data from memory to the USB.

The following table shows how the data direction corresponds to the USB token type in host and target device applications.

Table 24-4: Data Direction for USB Target Device

	RX	TX
Device	OUT or Setup	IN

24.6.4. Addressing Endpoint Buffer Table Entries

An understanding of the addressing mechanism of the Endpoint Buffer Table is useful when accessing endpoint data via the USB module or microprocessor. Some points of interest are:

- The Endpoint Buffer Table occupies up to 512 bytes of system memory.
- 16 bidirectional endpoints can be supported with a full EBT of 512 bytes.
- 16 bytes are needed for each USB endpoint direction.
- Applications with less than 16 endpoints require less RAM to implement the EBT.
- The EBT Page Registers point to the starting location of the EBT.
- The EBT must be located on a 512-byte boundary in system memory.
- All enabled TX and RX endpoint EB entries are indexed into the EBT to allow easy access via the USB module or CPU.

When a USB token on an enabled endpoint is received, the USB module uses its integrated DMA controller to

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interrogate the EBT. The USB SIE reads the corresponding endpoint EB entry to determine if it owns the EB entry and corresponding buffer in system memory.

To compute the entry point in the EBT, the EBT_PAGE registers is concatenated with the current endpoint and the TX and ODD fields to form a 32-bits address. This address mechanism is shown in the following diagrams:

Table 24-5: EBT Address Calculation Fields

Field	Description
EBT_PAGE	EBT_PAGE registers in the Control Register Block
END_POINT	END POINT field from the USB TOKEN
TX	1 for an TX transmit transfers and 0 for an RX receive transfers
ODD	This bit is maintained within the USB SIE. It corresponds to the buffer currently in use.
	The buffers are used in a ping-pong fashion.

24.6.5. Endpoint Buffer Table Formats

The Endpoint Buffer Table (EBT) provides endpoint control information for the USB module and microprocessor. The Endpoint Buffer Tables have different meaning based on whether it is the USB module or microprocessor reading the EB entry in memory.

The USB SIE Controller uses the data stored in the EB entrys to determine:

- Who owns the buffer in system memory
- Data0 or Data1 PID
- Release Own upon packet completion
- No address increment (FIFO Mode)
- Data toggle synchronization enable
- How much data is to be transmitted or received
- Where the buffer resides in system memory

While the microprocessor uses the data stored in the EB entrys to determine:

- Who owns the buffer in system memory
- Data0 or Data1 PID
- The received TOKEN PID
- How much data was transmitted or received
- Where the buffer resides in system memory

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The format for the EB entry is shown in the following figure.

Table 24-6: Endpoint Buffer Table Byte Format

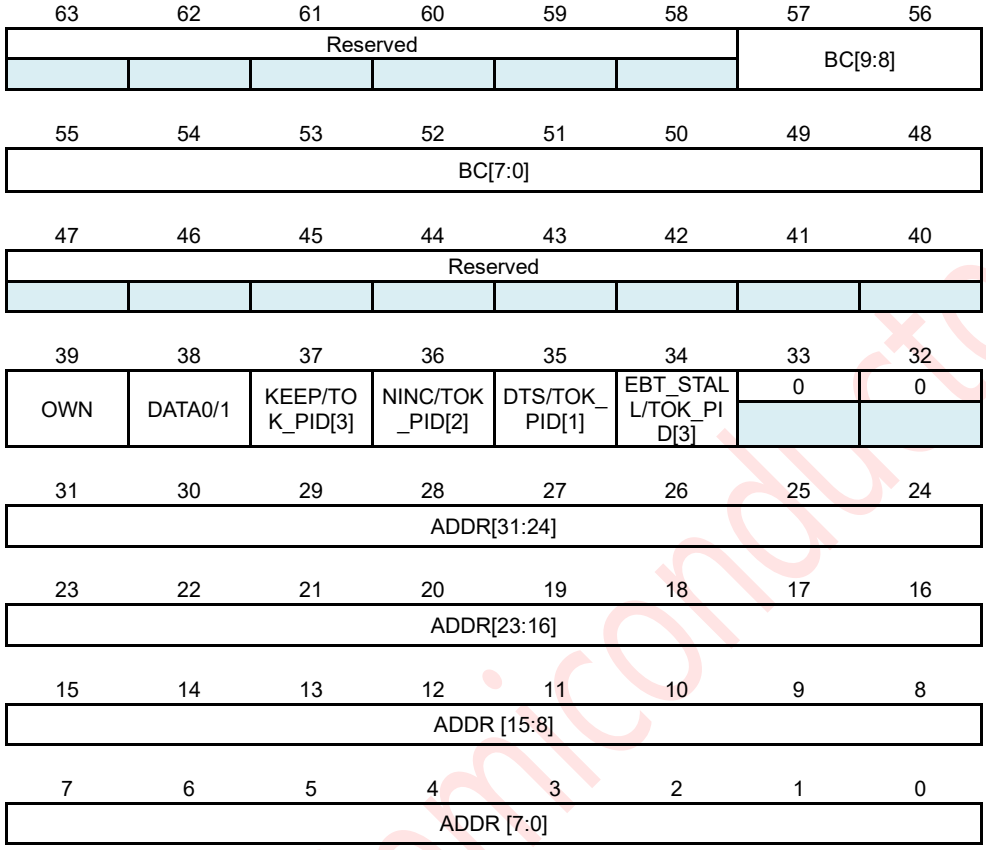


Table 24-7: Endpoint Buffer Table Byte Fields

Field	Description
OWN	**OWN** — This OWN bit determines who currently owns the buffer. Except when KEEP = 1, the USB SIE writes a 0 to this bit when it has completed a token. The USB module ignores all other fields in the EB entry when OWN = 0. Once the EB entry has been assigned to the USB module (OWN = 1), the MCU should not change it in any way. This byte of the EB entry should always be the last byte the MCU (firmware) updates when it initializes a EB entry. Although the hardware will not block the MCU from accessing the EB entry while owned by the USB SIE, doing so may cause undefined behavior and is generally not recommended. 0: The MCU has exclusive access to the entire EB entry 1: The USB module has exclusive access to the EB entry
DATA0/1	**Data Toggle** — This bit defines if a DATA0 field (DATA0/1 = 0) or a DATA1 (DATA0/1 = 1) field was transmitted or received. It is unchanged by the USB module. 0: Data 0 packet 1: Data 1 packet

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Field	Description
KEEP/ TOK_PID[3]	**KEEP / EB entry Token PID [3]** — Typically this bit is set (that is, 1) with ISO endpoints feeding a FIFO. The microprocessor is not informed that a token has been processed, the data is simply transferred to or from the FIFO. If KEEP is set, normally the NINC bit is also set to prevent address increment. 0: Bit 3 of the current token PID is written back in to the EB entry by the USB SIE. Allows the USB SIE to release the EB entry when a token has been processed. 1: This bit is unchanged by the USB SIE. If the OWN bit also is set, the EB entry remains owned by the USB SIE forever.
NINC/ TOK_PID[2]	**No Increment / EB entry Token PID [2]** — The No Increment (NINC) bit disables the DMA engine address increment. This forces the DMA engine to read or write from the same address. This is useful for endpoints when data needs to be read from or written to a single location such as a FIFO. Typically this bit is set with the KEEP bit for ISO endpoints that are interfacing to a FIFO. 0: The USB SIE writes bit 2 of the current token PID to the EB entry. 1: This bit is unchanged by the USB SIE.
DTS/ TOK_PID[1]	**Data Toggle Synchronization / EB entry Token PID [1]** — This bit enables data toggle synchronization. Setting this bit enables the USB SIE to perform Data Toggle Synchronization. • If KEEP = 0, bit 1 of the current token PID is written back to the EB entry. • If KEEP = 1, this bit is unchanged by the USB SIE. 0: No data toggle synchronization is performed. 1: Data toggle synchronization is performed.
EBT_STALL/ TOK_PID[0]	**EBT Stall / EB entry Token PID [0]** — Setting this bit will cause the USB module to issue a STALL handshake if a token is received by the SIE that would use the EBT in this location. The EBT is not consumed by the SIE (the OWN bit remains and the rest of the EB entry is unchanged) when the EBT_STALL bit is set. • If KEEP = 0, bit 0 of the current token PID is written back to the EB entry. • If KEEP = 1, this bit is unchanged by the USB SIE. 0: EBT stall is disabled 1: USB will issue a STALL handshake if a token is received by the SIE that would use the EBT in this location
TOK_PID[n]	Bits [37:34] can also represent the current token PID. The current token PID is written back in to the EB entry by the USB SIE when a transfer completes. The values written back are the token PID values from the USB specification: • 0x1 for an OUT token. • 0x9 for an IN token. • 0xD for a SETUP token.
BC[9:0]	**Byte Count** — The Byte Count bits represent the 10-bits byte count. The USB module serial interface engine (SIE) will change this field upon the completion of a RX transfer with the byte count of the data received.
ADDR[31:0]	The Address bits represent the 32-bits buffer address in system memory. These bits are unchanged by the USB SIE.

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24.6.6. USB Transaction

When the USB SIE transmits or receives data, it computes the EBT address using the address generation shown in "Addressing Endpoint Buffer Table Entries" table.

If OWN = 1, the following process occurs:

1. The USB SIE reads the EBT.
2. The SIE transfers the data via the DMA to or from the buffer pointed to by the ADDR field of the EB entry.
3. When the TOKEN is complete, the USB SIE updates the EBT and, if KEEP = 0, changes the OWN bit to 0.
4. The STAT register is updated and the TOK_DNE interrupt is set.
5. When the microprocessor processes the TOK_DNE interrupt, it reads from the status register all the information needed to process the endpoint.
6. At this point, the microprocessor allocates a new EB entry so additional USB data can be transmitted or received for that endpoint, and then processes the last EB entry.

The following figure shows a timeline of how a typical USB token is processed after the EBT is read and OWN = 1.

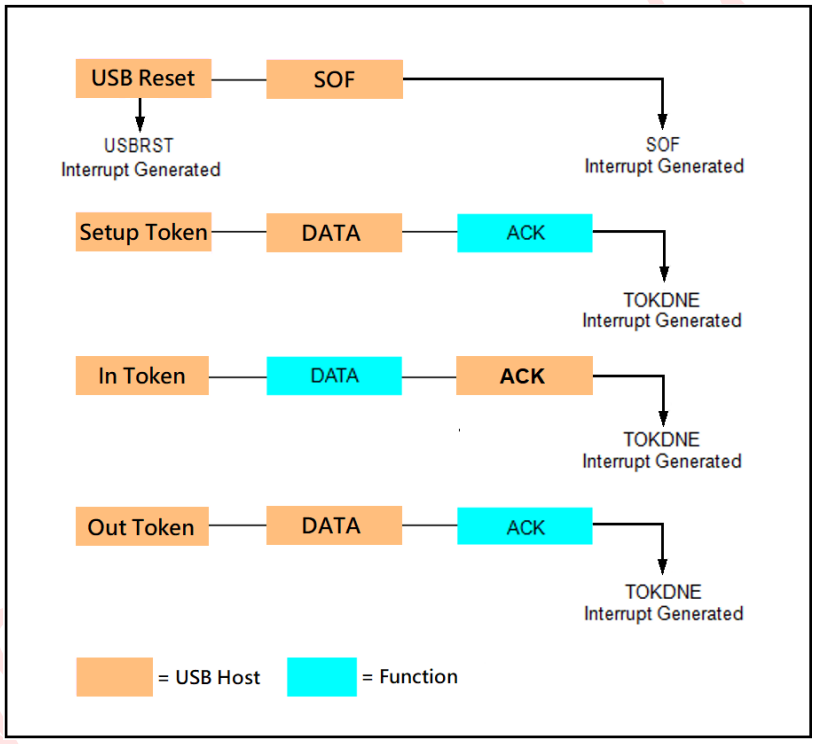


Figure 24-25: USB Token Transaction

The USB has two sources for the DMA overrun error:

Memory Latency

The memory latency on the DMA interface may be too high and cause the receive FIFO to overflow. This is predominantly a hardware performance issue, usually caused by transient memory access issues.

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Oversized Packets

The packet received may be larger than the negotiated MaxPacket size. Typically, this is caused by a software bug. For DMA overrun errors due to oversized data packets, the USB specification is ambiguous. It assumes correct software drivers on both sides. NAKing the packet can result in retransmission of the already oversized packet data. Therefore, in response to oversized packets, the USB core continues ACKing the packet for non-isochronous transfers.

Table 24-8: USB Responses to DMA Overrun Errors

Errors due to Memory Latency	Errors due to Oversized Packets
Non-Acknowledgment (NAK) or Bus Timeout (BTO) — See bit 4 in "Error Interrupt Status Register (ERR_STAT)" as appropriate for the class of transaction.	Continues acknowledging (ACKing) the packet for Nonisochronous transfers.
—	The data written to memory is clipped to the MaxPacket size so as not to corrupt system memory.
The DMA_ERR bit is set in the ERR_STAT register. Depending on the values of the INT_ENB and ERR_ENB register, the core may assert an interrupt to notify the processor of the DMA error.	Asserts the DMA_ERR bit of the ERR_STAT register (which could trigger an interrupt) and a TOK_DNE interrupt fires. **Note:** The TOK_PID field of the EBT is not 1111 because the DMA_ERR is not due to latency.
The EBT is not written back nor is the TOK_DNE interrupt triggered because it is assumed that a second attempt is queued and will succeed in the future.	The packet length field written back to the EBT is the MaxPacket value that represents the length of the clipped data actually written to memory.
From here, the software can decide an appropriate course of action for future transactions such as stalling the endpoint, canceling the transfer, disabling the endpoint, etc.	

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25. Analog-to-Digital Converter (ADC)

25.1. Introduction

The 12-bits ADC is a successive approximation analog-to-digital converter. It has up to 9 channels allowing it to measure signals from 8 external and 2 internal sources. A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The results of the ADC are stored in a 12-bits x 8 depth FIFO, and the data format can be left-aligned or right-aligned.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low power mode is implemented to allow very low consumption at low frequency.

25.2. ADC Main Features

- High Performance
  - 12-bits, 10-bits, 8-bits or 6-bits configurable resolution
  - ADC conversion time: 1.0 μs for 12-bits resolution (1MHz), 0.88 μs conversion time for 10-bits resolution, faster conversion times can be obtained by lowering resolution.
  - Programmable sampling time
  - Data alignment with built-in data coherency
  - DMA support
- Low Power
  - Application can reduce PLCK frequency for low power operation while still keeping optimum ADC performance. For example, 1.0 μs conversion time is kept, whatever the frequency of PCLK.
  - Wait mode: prevents ADC overrun in applications with low frequency PLCK
  - Auto off mode: ADC is automatically powered off except during the active conversion phase. This dramatically reduces the power consumption of the ADC.
- Analog Input Channels
  - 8 external analog inputs
  - 1 channel for internal reference voltage
  - 1 channel for internal temperature sensor
- Start-of-conversion can be initiated:
  - By software
  - By hardware triggers with configurable polarity
- Conversion Modes
  - Can convert a single channel or can scan a sequence of channels.
  - Single mode converts selected inputs once per trigger
  - Continuous mode converts selected inputs continuously
  - Discontinuous mode
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion, and in case of analog watchdog or overrun events.
- Analog Watchdog
- Single-ended and differential-input configurations
- Converter uses an internal reference or an external reference

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25.3. ADC Functional Description

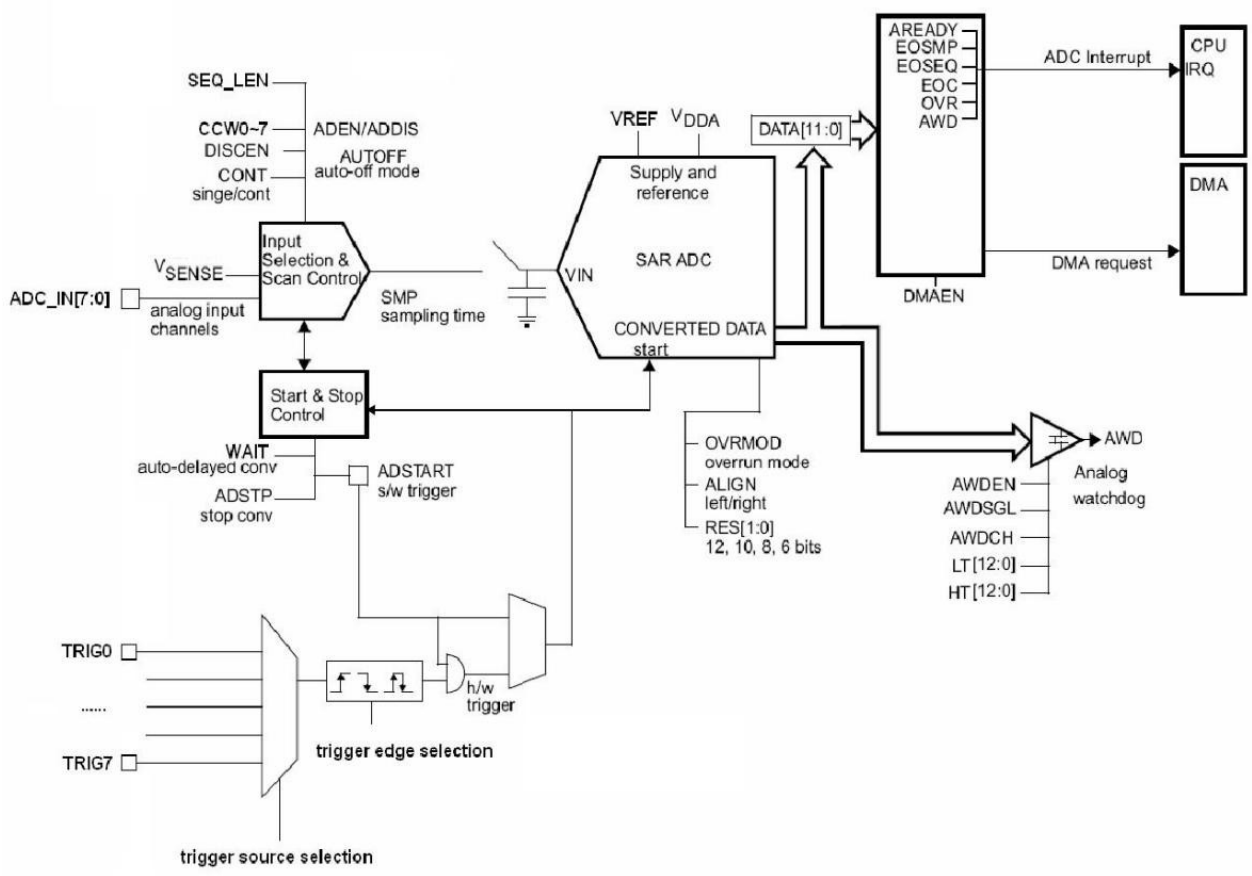


Figure 25-1: ADC Block Diagram

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25.3.1. ADC On-Off Control (ADEN, ADDIS, ADRDY)

At MCU power-up, the ADC is disabled and put in power-down mode (ADEN = 0) . As shown in **Figure 25-2**, the ADC needs a stabilization time of tSTAB(~2.0 µs) before it starts converting accurately.

Two control bits are used to enable or disable the ADC:

- Set ADEN = 1 to enable the ADC. The ADRDY flag is set as soon as the ADC is ready for operation.
- Set ADDIS = 1 to disable the ADC and put the ADC in power down mode. The ADEN and ADDIS bits are then automatically cleared by hardware as soon as the ADC is fully disabled.

Conversion can then start either by setting ADSTART = 1 or when an external trigger event occurs if triggers are enabled.

Follow this procedure to enable the ADC:

- Set ADEN = 1 in the ADC_CR register.
- Wait until ADRDY = 1 in the ADC_ISR register (ADRDY is set after the ADC startup time). This can be handled by interrupt if the interrupt is enabled by setting the ADRDYIE bit in the ADC_IER register.

Follow this procedure to disable the ADC:

- Check that ADSTART = 0 in the ADC_CR register to ensure that no conversion is ongoing. If required, stop any ongoing conversion by writing 1 to the ADSTP bit in the the ADC_CR register and waiting until this bit is read at 0.
- Set ADDIS = 1 in the ADC_CR register.
- If required by the application, wait until ADEN = 0 in the ADC_CR register, indicating that the ADC is fully disabled (ADDIS is automatically reset once ADEN = 0).

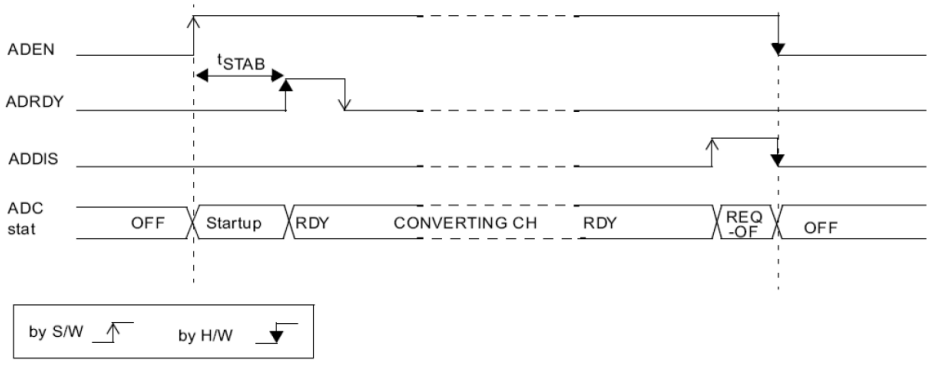


Figure 25-2: Enabling/Disabling the ADC

Note: In auto-off mode (AUTOFF = 1) the power-on/off phases are performed automatically, by hardware and the ADRDY flag is not set.

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25.3.2. ADC Clock

The ADC has a dual clock-domain architecture, as show in **Figure 25-3**, this has the advantage of reaching the maximum ADC clock frequency whatever the IPG clock scheme selected.

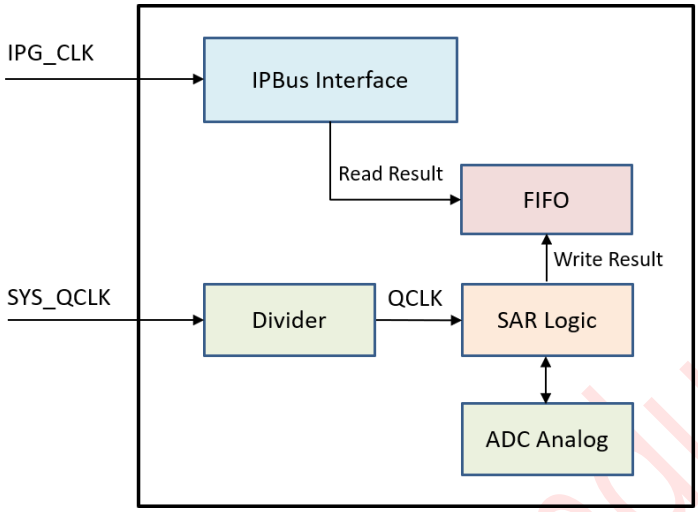


Figure 25-3: ADC Clock Scheme

25.3.3. Configuring The ADC

Software must write to the ADEN bit in the ADC_CR register if the ADC is disabled (ADEN must be 0).

Software must only write to the ADSTART and ADDIS bits in the ADC_CR register if the ADC is enabled and there is no pending request to disable the ADC (ADEN = 1 and ADDIS = 0).

For all the other control bits in the ADC_IER, ADC_CFGRi, ADC_SMPR, ADC_TR, ADC_CHSELRi and ADC_WDG registers, software must only write to the configuration control bits if there is no conversion ongoing (ADSTART = 0).

Software must only write to the ADSTP bit in the ADC_CR register if the ADC is enabled (and possibly converting) and there is no pending request to disable the ADC (ADSTART = 1 and ADDIS = 0) .

Note: There is no hardware protection preventing software from making write operations forbidden by the above rules. If such a forbidden write access occurs, the ADC may enter an undefined state. To recover correct operation in this case, the ADC must be disabled(ADDIS = 1).

25.3.4. Channel Selection (CCWi)

There are up to 10 multiplexed channels:

- 8 analog inputs from pins (ADC_IN0 ..... ADC_IN7)
- 2 internal analog input (VREFINT & Temperature Sensor)

It is possible to convert a single channel or to automatically scan a sequence of channels.

The sequence of the channels to be converted is organized as CCW[0], then CCW[1], ….. , then CCW[7]. The CCWi are programed in ADC_CHSELRi. The sequence length is programmed in SEQ_LEN[2:0] of ADC_CFGR2. For example, if sequence length is set as 3, then the sequence is organized as CCW[0], then CCW[1], then CCW[2].

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The channel decode is shown in **Table 25-1.**

Table 25-1: Channel Decode

CCWi[3:0]	Channel Select
4'b0000	ADC_IN0
4'b0001	ADC_IN1
4'b0010	ADC_IN2
4'b0011	ADC_IN3
4'b0100	ADC_IN4
4'b0101	ADC_IN5
4'b0110	ADC_IN6
4'b0111	ADC_IN7
4'b1110	VREFINT
4'b1111	Temperature Sensor

25.3.5. Programmable Sampling Time (SMP)

Before starting a conversion, the ADC needs to establish a direct connection between the voltage source to be measured and the embedded sampling capacitor of the ADC. This sampling time must be enough for the input voltage source to charge the sample and hold capacitor to the input voltage level.

Having a programmable sampling time allows to trim the conversion speed according to the input resistance of the input voltage source. The ADC samples the input voltage for a number of ADC clock cycles that can be modified using the SMP[3:0] bits in the ADC_SMPR register. This programmable sampling time is common to all channels.

The ADC indicates the end of the sampling phase by setting the EOSMP flag.

25.3.6. Single Conversion Mode (CONT = 0)

In Single conversion mode, the ADC converts the sequence once. This mode is selected when CONT = 0 in the ADC_CFGR1 register. Conversion is started by either:

- Setting the ADSTART bit in the ADC_CR register
- Hardware trigger event

Inside the sequence, after each conversion is complete:

- The converted data are stored in the FIFO
- The EOC (end of conversion) flag is set
- An interrupt is generated if the EOCIE bit is set

After the sequence of conversions is complete:

- The EOSEQ (end of sequence) flag is set
- An interrupt is generated if the EOSEQIE bit is set

Then the ADC stops until a new external trigger event occurs or the ADSTART bit is set again.

Note: To convert a single channel once, program a sequence with a length of 1.

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25.3.7. Continuous Conversion Mode (CONT = 1)

In continuous conversion mode, when a software or hardware trigger event occurs, the ADC performs a sequence of conversions, converting the sequence once and then automatically re-starts and continuously performs the same sequence of conversions. This mode is selected when CONT = 1 in the ADC_CFGR1 register. Conversion is started by either:

- Setting the ADSTART bit in the ADC_CR register
- Hardware trigger event

Inside the sequence, after each conversion is complete:

- The converted data are stored in the FIFO
- The EOC (end of conversion) flag is set
- An interrupt is generated if the EOCIE bit is set

After the sequence of conversions is complete:

- The EOSEQ (end of sequence) flag is set
- An interrupt is generated if the EOSEQIE bit is set

Then, a new sequence restarts immediately and the ADC continuously repeats the conversion sequence.

Note: It is not possible to have both discontinuous mode and continuous mode enabled: it is forbidden to set both bits DISCEN = 1 and CONT = 1.

25.3.8. Starting Conversions (ADSTART)

Software starts ADC conversions by setting ADSTART = 1.
When ADSTART is set, the conversion:

- Starts immediately if TRIGMODE = 0x0 (software trigger)
- At the next active edge of the selected hardware trigger if TRIGMODE ≠ 0x0

The ADSTART bit is also used to indicate whether an ADC operation is currently ongoing. It is possible to re-configure the ADC while ADSTART = 0, indicating that the ADC is idle.

The ADSTART bit is cleared by hardware:

- In single mode with software trigger
  _ At any end of conversion sequence (EOSEQ = 1)
- In discontinuous mode with software trigger
  _ At any end of conversion
- In all cases
  _ After execution of the ADSTP procedure invoked by software

Note:

- In continuous mode (CONT = 1), the ADSTART bit is not cleared by hardware when the EOSEQ flag is set because the sequence is automatically relaunched.
- When hardware trigger is selected in single mode, ADSTART is not cleared by hardware when the EOSEQ flag is set. This avoids the need for software having to set the ADSTART bit again and ensures the next trigger event is not missed.

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25.3.9. Timings

The elapsed time between the start of a conversion and the end of conversion is the sum of the configured sampling time plus the successive approximation time depending on data resolution:

tADC = tSMPL + tSAR = [4|min + 12|12-bits] x tQCLK = 1µs |min (for fQCLK = 16MHz)

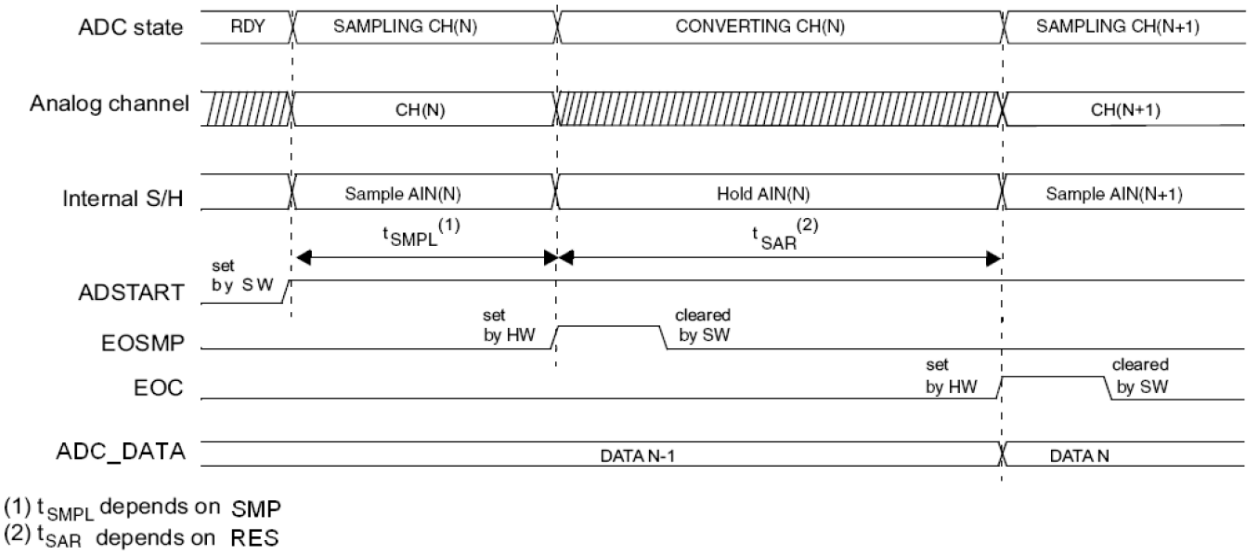


Figure 25-4: **Analog to Digital Conversion Time**

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25.3.10. Stopping An Ongoing Conversion (ADSTP)

The software can decide to stop any ongoing conversions by setting ADSTP = 1 in the ADC_CR register.

This will reset the ADC operation and the ADC will be idle, ready for a new operation.

When the ADSTP bit is set by software, any ongoing conversion is aborted and the result is discarded (FIFO is not updated with the current conversion). The scan sequence is also aborted and reset (meaning that restarting the ADC would re-start a new sequence).

Once this procedure is complete, the ADSTP and ADSTART bits are both cleared by hardware and the software must wait until ADSTART = 0 before starting new conversions.

Note: The flags in QADC_ISR are not cleared by STOP command, and the data in FIFO are not lost.

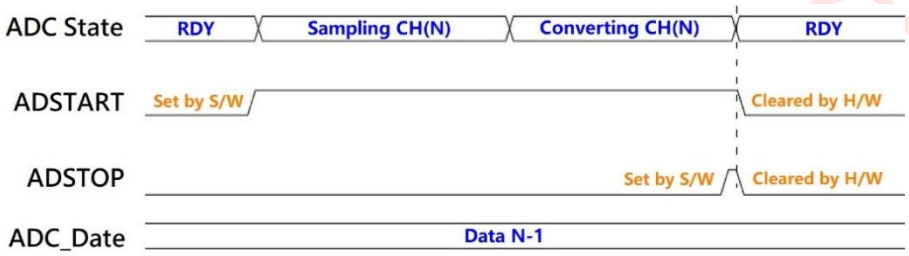


Figure 25-5: Stopping an Ongoing Conversion

25.4. Conversion On External Trigger And Trigger Polarity

A conversion or a sequence of conversion can be triggered either by software or by an external event. If the TRIGMODE control bits are not equal to “0”, then external events are able to trigger a conversion with the selected polarity. The trigger selection is effective once software has set bit ADSTART = 1.

Any hardware triggers which occur while a conversion is ongoing are ignored.

If bit ADSTART = 0, any hardware triggers which occur are ignored.

Table 25-2: Provides the correspondence between the TRIGMODE values and the trigger polarity.

Table 25-2: Configuring the Trigger Polarity.

TRIGMODE[2:0]	Source
3’b000	Trigger detection is disabled, software trigger
3’b001	Detection on rising edge
3’b010	Detection on falling edge
3’b011	Detection on both rising and falling edges
3’b100	Detection on high level voltage
3’b101	Detection on low level voltage
3’b110	Detection on PIT 0
3’b111	Detection on PWM 0

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Note:

The polarity of the external trigger can be changed only when the ADC is not converting (ADSTART = 0).

The TRIGSCR control bits are used to select which of 8 possible events can trigger conversions. **Table 25-3** gives the possible external trigger for regular conversion. Software source trigger events can be generated by setting the ADSTART bit in the ADC_CR register.

Table 25-3: Configuring the Trigger Polarity

TRIGSCR[2:0]	Name	Source
3'b000	TRG0	
3'b001	TRG1	
3'b010	TRG2	
3'b011	TRG3	
3'b100	TRG4	
3'b101	TRG5	
3'b110	TRG6	
3'b111	TRG7	

Note: The trigger selection can be changed only when the ADC is not converting (ADSTART = 0)

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25.4.1. Discontinuous Mode (DISCEN)

This mode is enabled by setting the DISCEN bit in the ADC_CFGR1 register.

In this mode (DISCEN = 1), a hardware or software trigger event is required to start each conversion defined in the sequence. On the contrary, if DISCEN = 0, a single hardware or software trigger event successively starts all the conversions defined in the sequence.

Example:

- DISCEN = 1, channels to be converted = 0, 3, 7, 10
  - 1st trigger: channel 0 is converted and an EOC event is generated
  - 2nd trigger: channel 3 is converted and an EOC event is generated
    Conversion on external trigger and trigger polarity (TRIGMODE, TRIGSCR)
  - 3rd trigger: channel 7 is converted and an EOC event is generated
  - 4th trigger: channel 10 is converted and both EOC and EOSEQ events are generated.
  - 5th trigger: channel 0 is converted an EOC event is generated
  - 6th trigger: channel 3 is converted and an EOC event is generated
  - ……..
- DISCEN = 0, channels to be converted = 0, 3, 7, 10
  - 1st trigger: the complete sequence is converted: channel 0, then 3, 7 and 10. Each conversion generates an EOC event and the last one also generates an EOSEQ event.
  - Any subsequent trigger events will restart the complete sequence.

25.4.2. Programmable Resolution (RES) - Fast Conversion Mode

It is possible to obtain faster conversion times (tSAR) by reducing the ADC resolution. The resolution can be configured to be either 12, 10, 8, or 6-bits by programming the RES[1:0] bits in the ADC_CFGR1 register. Lower resolution allows faster conversion times for applications where high data precision is not required.

Note:

The RES[1:0] bit must only be changed when the ADEN bit is reset.

The result of the conversion is always 13-bits wide and any unused LSB bits are read as zeroes.

Lower resolution reduces the conversion time needed for the successive approximation steps.

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25.4.3. End of Conversion, End of Sampling Phase (EOC, EOSMP Flags)

The ADC indicates each end of conversion (EOC) event.

The ADC sets the EOC flag in the ADC_ ISR register as soon as a new conversion data result is available. An interrupt can be generated if the EOCIE bit is set in the ADC_IER register. The EOC flag is cleared by software either by writing 1 to it, or by reading the FIFO.

The ADC also indicates the end of sampling phase by setting the EOSMP flag in the ADC_ISR register. The EOSMP flag is cleared by software by writing 1 to it. An interrupt can be generated if the EOSMPIE bit is set in the ADC_IER register.

25.4.4. End Of Conversion Sequence (Eoseq Flag)

The ADC notifies the application of each end of sequence (EOSEQ) event.

The ADC sets the EOSEQ flag in the ADC_ISR register as soon as the last data result of a conversion sequence is available in the FIFO. An interrupt can be generated if the EOSEQIE bit is set in the ADC_IER register. The EOSEQ flag is cleared by software by writing 1 to it.

25.4.5. Example Timing Diagrams

This section shows the single and continuous modes in hardware or software triggers condition.

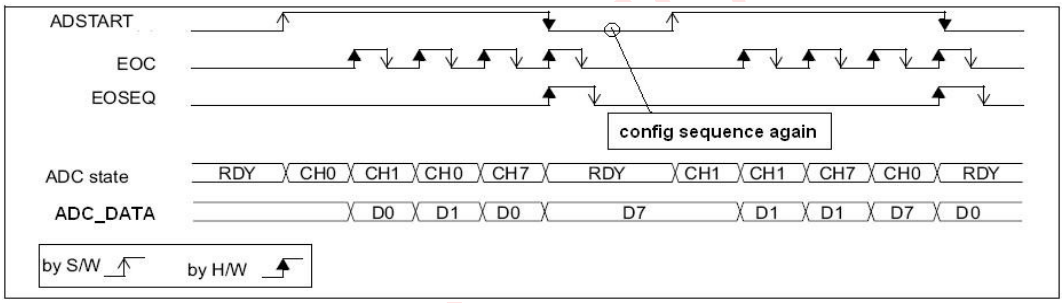


Figure 25-6: **Single conversions of a sequence, software trigger**

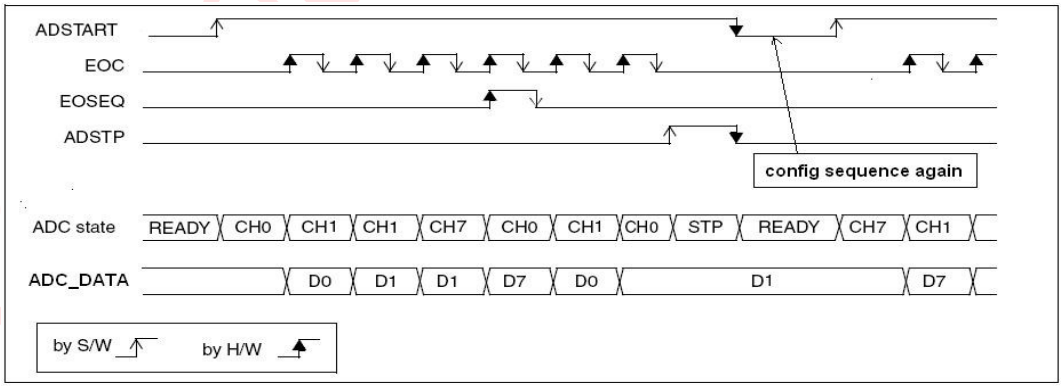


Figure 25-7: **Continuous Conversion of a Sequence, Software Trigger**

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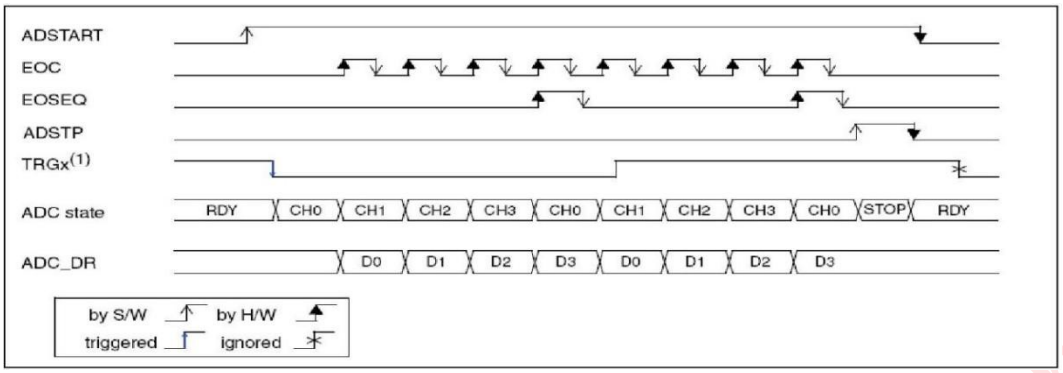


Figure 25-8: **Single Conversions of a Sequence, Hardware Trigger**

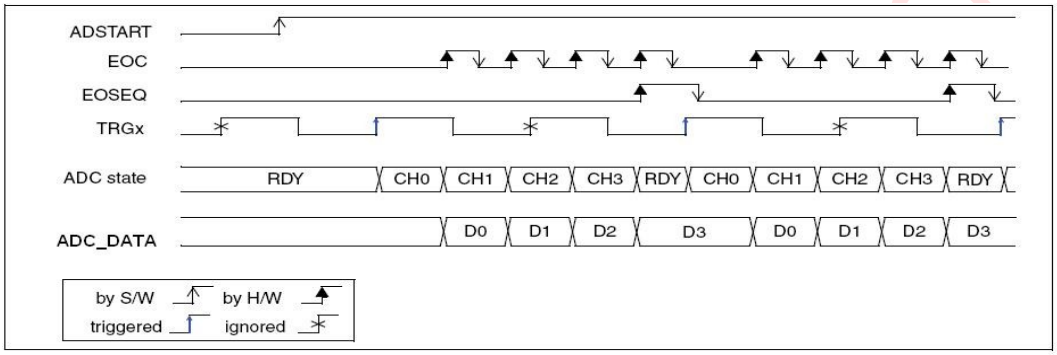


Figure 25-9: **Continuous Conversions of a Sequence, Hardware Trigger**

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25.5. Data Management

25.5.1. Data FIFO & Data Alignment (ADC_FIFO, ALIGN)

At the end of each conversion (when an EOC event occurs), the result of the converted data is stored in the ADC_FIFO which is 13-bits wide x 8 depth.

The format of the read out data depends on the configured data alignment and resolution.

The ALIGN bit in the ADC_CFGR1 register selects the alignment of the data stored after conversion. Data can be right-aligned (ALIGN = 0) or left-aligned (ALIGN = 1) as shown in **Table 25-4.**

Table 25-4: Data Alignment and Resolution

Align	RES[1:0]	31	30	….	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0x0			….					Data[11:0]											
	0x1			….							Data[9:0]									
	0x2			….									Data[7:0]							
	0x3			….											Data[5:0]					
1	0x0			….	Data[11:0]															
	0x1			….	Data[9:0]															
	0x2			….									Data[7:0]							
	0x3			….									Data[5:0]							

The FIFO supports byte, half-word and word read, but the address offset should be always 0x4C.
For different data alignments and resolutions, users should note:

- If read by word, then the data format is as data[31:0] as **Table 25-4** shows
- if read by half word, then the data format is as data[15:0] as **Table 25-4** shows
- If read by byte when the data is longer than 8-bits, then the high byte is first read out, and the low byte should read again.
- If read by byte when the data is not longer than 8-bits, then the data format is as data[7:0] as **Table 25-4** shows.

25.5.2. ADC Overrun (OVR, OVRMOD)

The overrun flag (OVR) indicates a data overrun event, when the converted data was not read in time by the CPU or the DMA, before the FIFO is full.

The OVR flag is set in the ADC_ISR register if the FULL flag is still at '1' at the time when a new conversion completes. An interrupt can be generated if the OVRIE bit is set in the ADC_IER register.

When an overrun condition occurs, the ADC keeps operating and can continue to convert unless the software decides to stop and reset the sequence by setting the ADSTP bit in the ADC_CR register.

The OVR flag is cleared by software by writing 1 to it.

It is possible to configure if the data is preserved or overwritten when an overrun event occurs by programming the OVRMOD bit in the ADC_CFGR1 register:

•OVRMOD = 0

– An overrun event preserves the data register from being overwritten: the old data is maintained and the new conversion is discarded. If OVR remains at 1, further conversions can be performed but the resulting data is discarded.

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•OVRMOD = 1

– The data register is overwritten with the last conversion result. If OVR remains at 1, further conversions can be performed and the FIFO always contains the data from the latest conversion.

25.5.3. Managing A Sequence Of Data Converted Without Using The DMA

If the conversions are slow enough, the conversion sequence can be handled by software. In this case the software can use the EOC flag and its associated interrupt to handle each data result. Each time a conversion is complete, the EOC bit is set in the ADC_ISR register and the FIFO register can be read.

Software can also use FIFO EMPTY flag to handle each data result. If EMPTY is not "0", this means FIFO has new data.

The OVRMOD bit in the ADC_CFGR1 register should be configured to 0 to manage overrun events as an error.

25.5.4. Managing Converted Data Without Using The DMA Without Overrun

It may be useful to let the ADC convert one or more channels without reading the data after each conversion. In this case, the OVRMOD bit must be configured at 1 and the OVR flag should be ignored by the software. When OVRMOD = 1, an overrun event does not prevent the ADC from continuing to convert and the FIFO always contains the latest conversion data.

25.5.5. Managing Converted Data Using The DMA

Once the data number in the FIFO is not empty and bit DMAEN is set, QADC will send request to the DMA. This allows the transfer of the converted data from the FIFO to the destination location selected by the software.

Despite this, if an overrun occurs (OVR = 1) because the DMA could not serve the DMA transfer request in time, the ADC stops generating DMA requests and the data corresponding to the new conversion is not transferred by the DMA. This means that all the data transferred to the RAM can be considered as valid.

Depending on the configuration of OVRMOD bit, the data is either preserved or overwritten.

The DMA transfer requests are blocked until the software clears the OVR bit.

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25.6. Low Power Features

25.6.1. Wait Mode Conversion

Wait mode conversion can be used to simplify the software as well as optimizing the performance of applications clocked at low frequency where there might be a risk of ADC overrun occurring. When the WAIT bit is set to 1 in the ADC_CFGR1 register, a new conversion can start only if the FIFO is not full.

This is a way to automatically adapt the speed of the ADC to the speed of the system that reads the data.

Note: Any hardware triggers which occur while a conversion is ongoing or during the wait time preceding the read access are ignored.

25.6.2. Auto-off Mode (AUTOFF)

The ADC has an automatic power management feature which is called auto-off mode, and is enabled by setting AUTOFF = 1 in the ADC_CFGR1 register.

When AUTOFF = 1, the ADC is always powered off when not converting and automatically wakes-up when a conversion is started (by software or hardware trigger). A startup-time is automatically inserted between the trigger event which starts the conversion and the sampling time of the ADC. The ADC is then automatically disabled once the sequence of conversions is complete.

Auto-off mode can cause a dramatic reduction in the power consumption of applications which need relatively few conversions or when conversion requests are timed far enough apart (for example, with a low frequency hardware trigger) to justify the extra power and extra time used for switching the ADC on and off.

Auto-off mode can be combined with the wait mode conversion (WAIT = 1) for applications clocked at low frequency. This combination can provide significant power savings if the ADC is automatically powered-off during the wait phase and restarted as soon as the FIFO is read by the application

25.7. Analog Window Watchdog (AWD)

The AWD analog watchdog feature is enabled by setting the AWDEN bit in the ADC_CFGR1 register. It is used to monitor that either one selected channel or all enabled channels remain within a configured voltage range (window) as shown in **Figure 25-10**.

The AWD analog watchdog status bit is set if the analog voltage converted by the ADC is below a lower threshold or above a higher threshold. These thresholds are programmed in the ADC_TR register. An interrupt can be enabled by setting the AWDIE bit in the ADC_IER register.

The AWD flag is cleared by software by writing 1 to it.

When converting a data with a resolution of less than 12-bits (according to bits RES[1:0]), the LSB of the programmed thresholds must be kept cleared because the internal comparison is always performed on the full 12-bits raw converted data (left aligned).

Table 25-5 shows how to configure the AWDSGL and AWDEN bits in the ADC_CFGR1 register to enable the analog watchdog on one or more channels.

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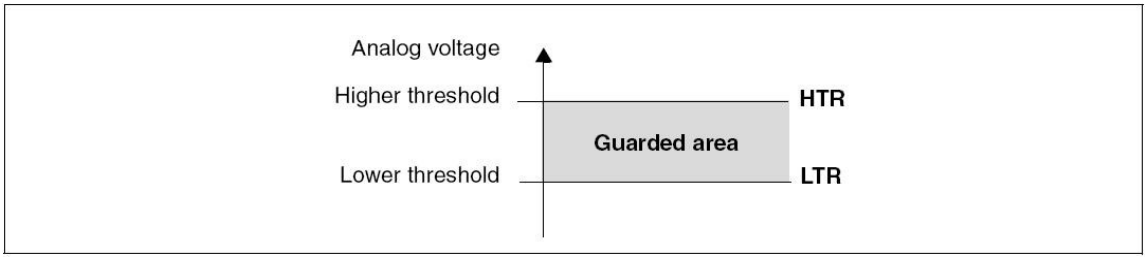


Figure 25-10: Analog Watchdog Guarded Area

Table 25-5: Analog Watchdog Channel Selection

Channels Guarded by the Analog Watchdog	AWDSGL Bit	AWDEN Bit
None	X	0
All Channel	0	1
Single (1) Channel	1	1

Note (1) : Selected by the AWDCH

25.8. Temperature Sensor

The temperature sensor is internally connected to the ADC1_IN15 input channel which is used to convert the sensor's output voltage to a digital value.

25.9. ADC Interrupts

An interrupt can be generated by any of the following events:

- •ADC power-up, when the ADC is ready (ADRDY Flag)
- •End of any conversion (EOC Flag)
- •End of a sequence of conversions (EOSEQ Flag)
- •When an analog watchdog detection occurs (AWD Flag)
- •When the end of sampling phase occurs (EOSMP Flag)
- •When a data overrun occurs (OVR flag) Separate interrupt enable bits are available for flexibility.

Table 25-6: ADC Interrupts

Interrupt Event	Event Flag	Enable Control Bit
ADC Ready	ADRDY	ADRDYIE
End of Conversion	EOC	1EOCIE
End of Sequence of Conversions	EOSEQ	1EOSEQIE
Analog Watchdog Status bit is Set	AWD	AWDIE
End of Sampling Phase	EOSMP	EOSMPIE
Overrun	OVR	OVRIE

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25.10. Memory Map and Registers

The ADC Module memory map is shown in **Table 25-7**. The ADC base address is 0x4011_0000. This subsection describes the memory map and register structure of ADC.

25.10.1. Memory Map

Refer to **Table 25-7** for a description of the QADC memory map.

Table 25-7: **ADC Module Memory Map**

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ADC_ISR																									AWD	Empty	FULL	OVR	EOSEQ	EOC	EOSMP	ADRDY
0x04	ADC_IER																									AWDIE			OVRIE	EOSEQIE	EOCIE	EOSMPIE	ADRDYIE
0x08	ADC_CR																													ADSTP	ADSTART	ADDIS	ADEN
0x0C	ADC_CFGR1	DIFF	OVRMOD				SEQLEN[2:0]			DISCEN	AUTOFF	WAIT	CONT		TRIGSCR[2:0]					TRIGMODE[2:0]		ALIGN	RES[1:0]										DMAEN
0x10	ADC_CFGR2																					QPR[3:0]				STCNT[7:0]							
0x14	ADC_SMPR																									SMP[7:0]							
0x18	ADC_WDG																									AWDEN	AWDSGL			AWDCH[3:0]			
0x1C	ADC_TR					HT[11:0]																LT[11:0]											
0x2C	ADC_CHSELR1					CCW3[3:0]								CCW2[3:0]								CCW1[3:0]							CCW0[3:0]			
0x30	ADC_CHSELR2					CCW7[3:0]								CCW6[3:0]								CCW5[3:0]							CCW4[3:0]			
0x4C	ADC_FIFO																	DATA[15:0]															

Note: 1. All the registers are CPU supervisor or user mode accessable.

2. The darked bits are reserved, and must be kept at reset value.

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25.10.2. Register Descriptions

25.10.2.1. ADC Interrupt And Status Register (ADC_ISR)

Address: ADC_BASEADDR+0x0000_0000

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	AWD	EMPTY	FULL	OVR	EOSEQ	EOC	EOSMP	ADRDY
Write:	w1c			w1c	w1c	w1c	w1c	w1c
Reset:	0	1	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

w1c = .Write 1 to the bit will clear it

Figure 25-11: ADC Interrupt and Status Register (ADC_ISR)

Read: Anytime

Write: Anytime

AWD — Analog watchdog flag

This bit is set by hardware when the converted voltage crosses the values programmed in the ADC_TR register. It is cleared by software writing 1 to it.

1 = Analog watchdog event occurred

0 = No analog watchdog event occurred (or the flag event was already acknowledged and cleared by software)

EMPTY — FIFO empty status

This bit is set by hardware when the FIFO is empty. It is cleared by hardware when FIFO is not empty.

1 = FIFO is empty

0 = FIFO is not empty

FULL — FIFO full status

This bit is set by hardware when the FIFO is full. It is cleared by hardware when FIFO is not full.

1 = FIFO is full

0 = FIFO is not full

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OVR — ADC overrun

This bit is set by hardware when an overrun occurs, meaning that a new conversion has complete while the FULL flag was already set. It is cleared by software writing 1 to it.

1 = Overrun has occurred

0 = No overrun occurred (or the flag event was already acknowledged and cleared by software)

EOSEQ — End of sequence flag

This bit is set by hardware at the end of the conversion of a sequence. It is cleared by software writing 1 to it.

1 = Conversion sequence complete

0 = Conversion sequence not complete (or the flag event was already acknowledged and cleared by software)

EOC — End of conversion flag

This bit is set by hardware at the end of each conversion of a channel when a new data result is available in the ADC_FIFO register. It is cleared by software writing 1 to it or by reading the ADC_FIFO register.

1 = Channel conversion complete

0 = Channel conversion not complete (or the flag event was already acknowledged and cleared by software)

EOSMP — End of sampling flag

This bit is set by hardware during the conversion, at the end of the sampling phase.

1 = End of sampling phase reached

0 = Not at the end of the sampling phase (or the flag event was already acknowledged and cleared by software)

ADRDY — ADC ready

This bit is set by hardware after the ADC has been enabled (bit ADEN = 1) and when the ADC reaches a state where it is ready to accept conversion requests. It is cleared by software writing 1 to it.

1 = ADC is ready to start conversion

0 = ADC not yet ready to start conversion (or the flag event was already acknowledged and cleared by software)

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25.10.2.2. ADC Interrupt Enable Register (ADC_IER)

Address: ADC_BASEADDR+0x0000_0004

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	AWDIE	0	0	OVRIE	EOSEQIE	EOCIE	EOSMPIE	ADRDYIE
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 25-12: ADC Interrupt Enable Register (ADC_IER)

Read: Anytime

Write: Before ADC start

AWDIE — Analog watchdog interrupt enable

This bit is set and cleared by software to enable/disable the analog watchdog interrupt.

1 = Analog watchdog interrupt is enabled

0 = Analog watchdog interrupt is disabled

OVRIE — Overrun interrupt enable

This bit is set and cleared by software to enable/disable the overrun interrupt.

1 = Overrun interrupt is enabled. An interrupt is generated when the OVR bit is set.

0 = Overrun interrupt is disabled

EOSEQIE — End of conversion sequence interrupt enable

This bit is set and cleared by software to enable/disable the end of sequence of conversions interrupt.

1 = EOSEQ interrupt is enabled. An interrupt is generated when the EOSEQ bit is set.

0 = EOSEQ interrupt is disabled

EOCIE — End of conversion interrupt enable

This bit is set and cleared by software to enable/disable the end of conversion interrupt.

1 = EOC interrupt is enabled. An interrupt is generated when the EOC bit is set.

0 = EOC interrupt is disabled

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EOSMPIE — End of sampling flag interrupt enable

This bit is set and cleared by software to enable/disable the end of the sampling phase interrupt.

1 = EOSMP interrupt is enabled. An interrupt is generated when the EOSMP bit is set.

0 = EOSMP interrupt is disabled.

ADRDYIE — ADC ready interrupt enable

This bit is set and cleared by software to enable/disable the ADC Ready interrupt.

1 = ADRDY interrupt is enabled. An interrupt is generated when the ADRDY bit is set.

0 = ADRDY interrupt is disabled.

25.10.2.3. ADC Control Register (ADC_CR)

Address: ADC_BASEADDR+0x0000_0008

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	1	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0				ADSTP	ADSTART	ADDIS	ADEN
Write:					rs	rs	rs	rs
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

rs = Software can read and set, write 0 has no effect

Figure 25-13: ADC Control Register (ADC_CR)

Read: Anytime

Write: See each bit description

ADSTP — ADC stop conversion command

This bit is set by software to stop and discard an ongoing conversion (ADSTP Command). It is cleared by hardware when the conversion is effectively discarded and the ADC is ready to accept a new start conversion command.

1 = Write 1 to stop the ADC. Read 1 means that an ADSTP command is in progress.

0 = No ADC stop conversion command ongoing

Note: Software is allowed to set ADSTP only when ADSTART = 1 and ADDIS = 0 (ADC is enabled and may be converting and there is no pending request to disable the ADC)

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ADSTART — ADC start conversion command

This bit is set by software to start ADC conversion. Depending on the TRIGMODE configuration bits, a conversion either starts immediately (software trigger configuration) or once a hardware trigger event occurs (hardware trigger configuration).

It is cleared by hardware:

– In single conversion mode when software trigger is selected: at the assertion of the End of Conversion Sequence (EOSEQ) flag.

– In discontinued conversion mode when software trigger is selected: at the assertion of the End of Conversion (EOC) flag.

– In all cases: after the execution of the ADSTP command, at the same time as the ADSTP bit is cleared by hardware.

1 = Write 1 to start the ADC. Read 1 means that the ADC is operating and may be converting.

0 = No ADC conversion is ongoing.

Note: Software is allowed to set ADSTART only when ADEN = 1 and ADDIS = 0 (ADC is enabled and there is no pending request to disable the ADC)

ADDIS — ADC disable command

This bit is set by software to disable the ADC (ADDIS command) and put it into power-down state (OFF state). It is cleared by hardware once the ADC is effectively disabled (ADEN is also cleared by hardware at this time).

1 = Write 1 to disable the ADC. Read 1 means that an ADDIS command is in progress.

0 = No ADDIS command ongoing

Note: Software is allowed to set ADDIS only when ADEN = 1 and ADSTART = 0 (which ensures that no conversion is ongoing)

ADEN — ADC enable command

This bit is set by software to enable the ADC. The ADC will be effectively ready to operate once the ADRDY flag has been set. It is cleared by hardware when the ADC is disabled, after the execution of the ADDIS command.

1 = Write 1 to enable the ADC.

0 = ADC is disabled (OFF state) .

Note: Software is allowed to set ADEN only when all bits of ADC_CR registers are 0 (ADSTP = 0, ADSTART = 0, ADDIS = 0 and ADEN = 0)

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25.10.2.4. ADC Configuration Register 1 (ADC_CFGR1)

Address: ADC_BASEADDR+0x0000_000C

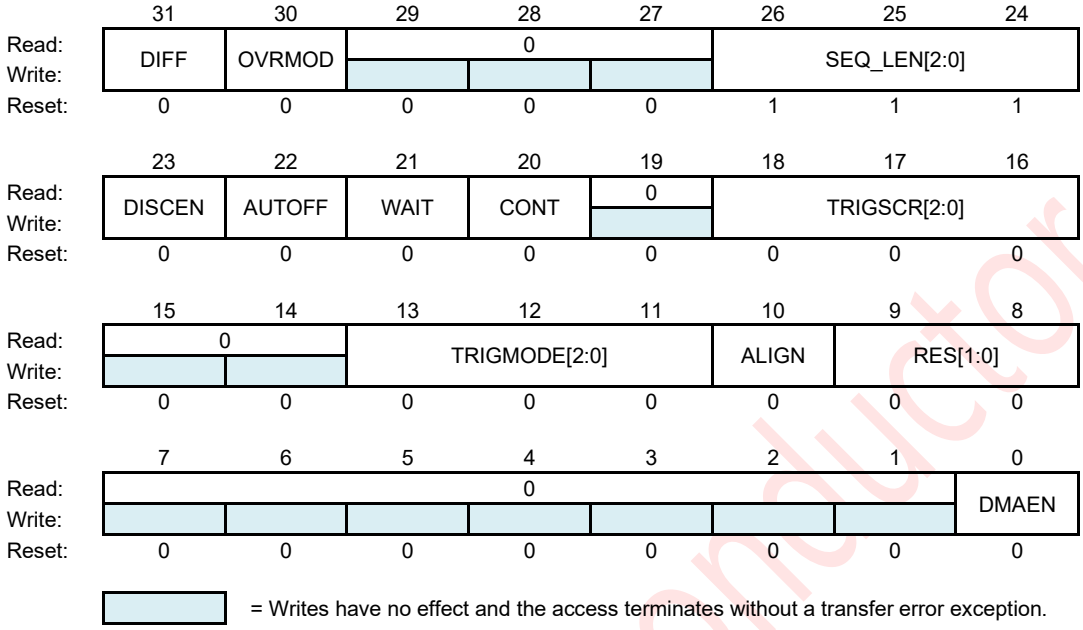


Figure 25-14: ADC Configuration Register 1 (ADC_CFGR1)

Read: Anytime

Write: Before ADC start

DIFF — Select differential-input

This bit determines that if the input is single-ended or differential-input.

1 = The analog input is differentially sampled.

0 = The analog input is single sampled

OVRMOD — Overrun management mode

This bit is set and cleared by software and configures the way data overruns are managed.

1 = ADC_DR register is overwritten with the last conversion result when an overrun is detected.

0 = ADC_DR register is preserved with the old data when an overrun is detected.

SEQ_LEN[2:0] — Sequence length

These bits define the length of sequence. The sequence length = SEQ_LEN+1. For example, SEQ_LEN = 7 means sequence length is 8; SEQ_LEN = 0 means sequence length is 1.

DISCEN — Discontinuous mode

This bit is set and cleared by software to enable/disable discontinuous mode.

1 = Discontinuous mode is enabled

0 = Discontinuous mode is disabled

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AUTOFF — Auto-off mode

This bit is set and cleared by software to enable/disable auto-off mode.

1 = Auto-off mode is enabled

0 = Auto-off mode is disabled

WAIT — Wait conversion mode

This bit is set and cleared by software to enable/disable wait conversion mode.

1 = Wait conversion mode on

0 = Wait conversion mode off

CONT — Single / continuous conversion mode

This bit is set and cleared by software. If it is set, conversion takes place continuously until it is cleared

1 = Continuous conversion mode

0 = Single conversion mode

TRIGSCR[2:0] — External trigger source

These bits are used to select which of 8 possible events can trigger conversions.

See **Table 25-3.**

TRIGMODE[2:0] — Trigger mode select

These bits are used to select software trigger mode or external trigger polarity, see **Table 25-2**.

ALIGN — Data alignment

This bit is set and cleared by software to select right or left alignment. Refer to **Table 25-4**.

0 = Right alignment

1 = Left alignment

RES[1:0] — Data resolution

These bits are written by software to select the resolution of the conversion. Refer to **Table 25-4**.

DMAEN — Direct memory access enable

This bit is set and cleared by software to enable the generation of DMA requests. This allows to use the DMA controller to manage automatically the converted data.

1 = DMA is enabled

0 = DMA is disabled

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25.10.2.5. ADC Configuration Register 2 (ADC_CFGR2)

Address: ADC_BASEADDR+0x0000_0010

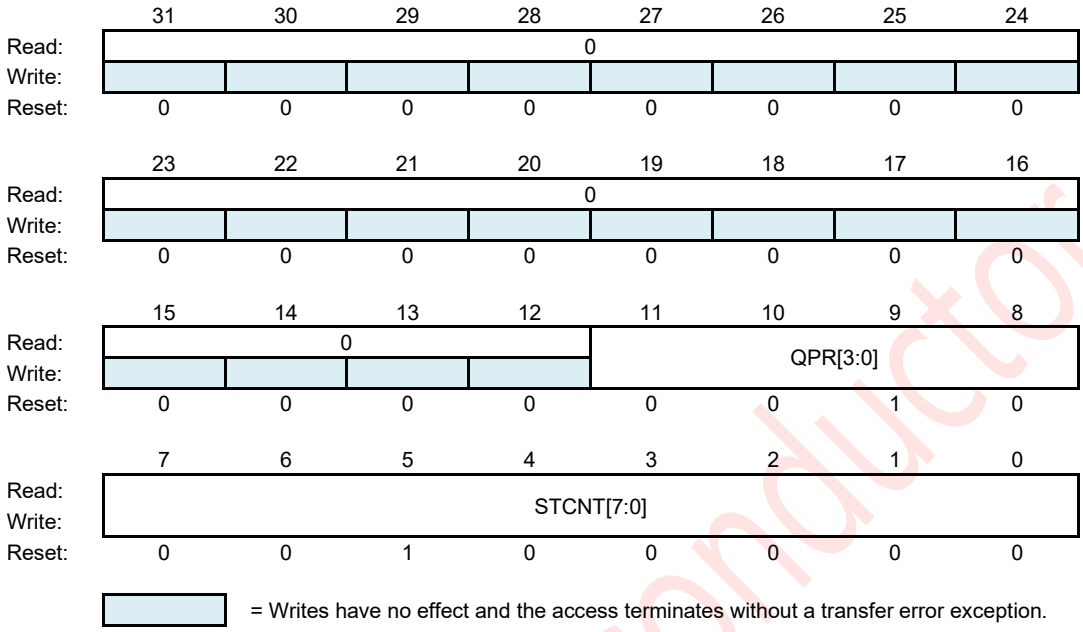


Figure 25-15: ADC Configuration Register 2 (ADC_CFGR2)

Read: Anytime

Write: Before ADC enable

QPR[3:0] — Prescaler Clock Divider Bits

These bits select the system clock divisor to generate the QADC clock as follows:

FQCLK = Fsys_QCLK / (QPR[3:0] + 1)

where:

0 < QPR[3:0] <= 15 and the value 1 is not allowed.

STCNT[7:0] — ADC startup counter bits

The ADC needs a stabilization time of tSTAB(~2us) before it starts converting accurately. This time is calculated by counting QCLK cycles until the internal counter reachs the STCNT[7:0]. So user should set these bits before ADC enable. For example, if the QCLK = 16MHz, then users should set the STCNT[7:0] = 2000/(1000/16) = 32.

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25.10.2.6. ADC Sampling Time Register (ADC_SMPR)

Address: ADC_BASEADDR+0x0000_0014

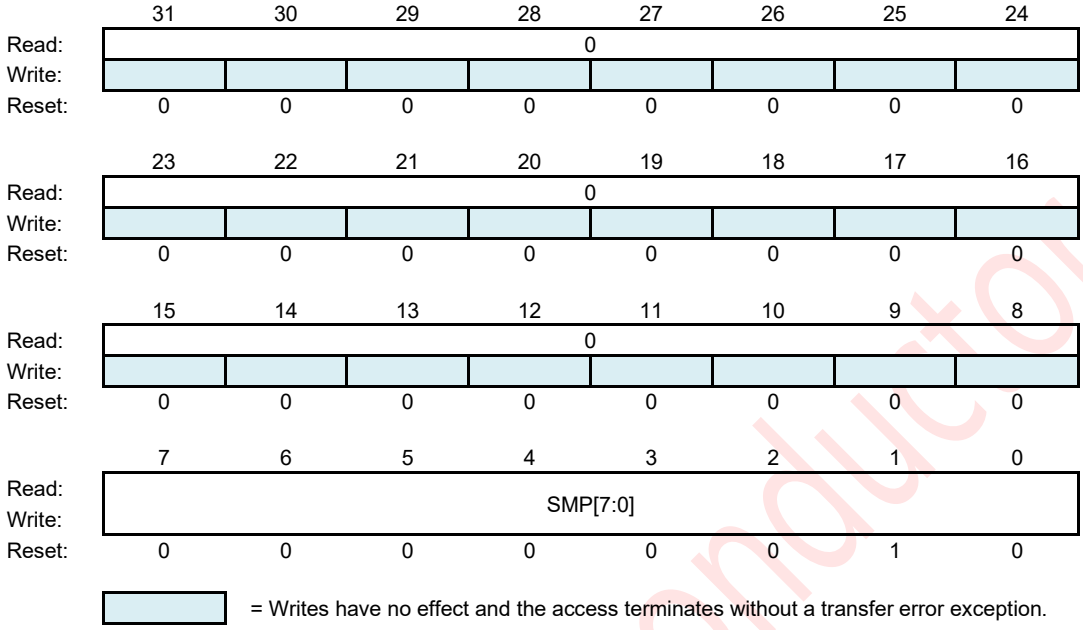


Figure 25-16: ADC Sampling Time Register (ADC_SMPR)

Read: Anytime

Write: Before ADC start

SMP[7:0] — Sampling time selection

These bits are written by software to select the sampling time that applies to all channels. The sample time is calculated as (SMP[7:0]+2) QCLKs

Example: SMP[7:0] = 0x2 means the sample time is 4 QCLKs

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25.10.2.7. ADC Watch Dog Register (ADC_WDG)

Address: ADC_BASEADDR+0x0000_0018

	31	30	29	28	27	26	25	24
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0							
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	AWDEN	AWDSGL	0	0	AWDCH[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 25-17: ADC Watchdog Register (ADC_WDG)

Read: Anytime

Write: Before ADC start

AWDEN — Analog watchdog enable

This bit is set and cleared by software.

1 = Analog watchdog is enabled

0 = Analog watchdog is disabled

AWDSGL — Enable the watchdog on a single channel or on all channels

This bit is set and cleared by software to enable the analog watchdog on the channel identified by the AWDCH[4:0] bits or on all the channels

1 = Analog watchdog is enabled on a single channel

0 = Analog watchdog is enabled on all channels

AWDCH[3:0] — Analog watchdog channel selection

These bits are set and cleared by software. They select the input channel to be guarded by the analog watchdog.

- 0000: ADC analog input Channel 0 monitored by AWD
- 0001: ADC analog input Channel 1 monitored by AWD
- .....
- .....
- .....
- 0111: ADC analog input Channel 7 monitored by AWD
- 1111: Temperature sensor monitored by AWD
- other values: Reserved, must not be used

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25.10.2.8. ADC Watchdog Threshold Register (ADC_TR)

Address: ADC_BASEADDR+0x0000_001C

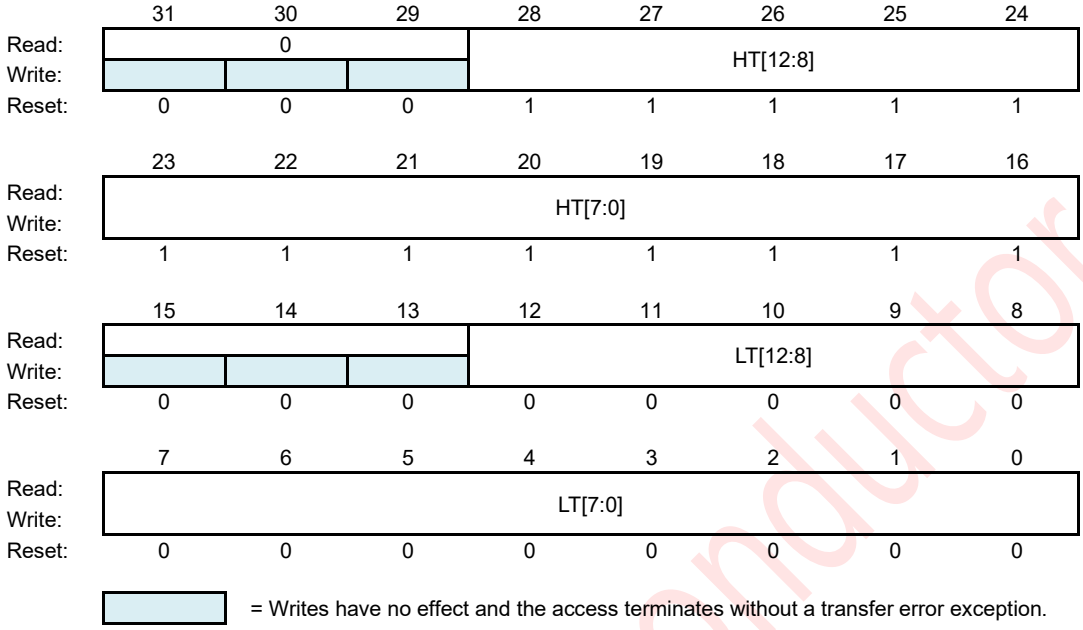


Figure 25-18: **ADC Watchdog Threshold Register (ADC_TR)**

Read: Anytime

Write: Before ADC start

HT[12:0] — Analog watchdog higher threshold
These bits are written by software to define the higher threshold for the analog watchdog.

LT[12:0] — Analog watchdog lower threshold
These bits are written by software to define the lower threshold for the analog watchdog.

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25.10.2.9. ADC Channel Selection Register (ADC_CHSELR)

Address: ADC_BASEADDR+0x0000_002C

	31	30	29	28	27	26	25	24
Read:	0				CCW3[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0				CCW2[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0				CCW1[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0				CCW0[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 25-19: ADC Channel Selection Register 1(ADC_CHSELR1)

Address: ADC_BASEADDR+0x0000_0030

	31	30	29	28	27	26	25	24
Read:	0				CCW7[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

	23	22	21	20	19	18	17	16
Read:	0				CCW6[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Read:	0				CCW5[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
Read:	0				CCW4[3:0]			
Write:								
Reset:	0	0	0	0	0	0	0	0

= Writes have no effect and the access terminates without a transfer error exception.

Figure 25-20: ADC Channel Selection Register 2(ADC_CHSELR2)

Read: Anytime

Write: Before ADC start

CCWx[3:0] — The number x conversion select channel, refer to **Table 25-1**.

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25.10.2.10. ADC FIFO Access Register (ADC_FIFO)

Address: ADC_BASEADDR+0x0000_004C

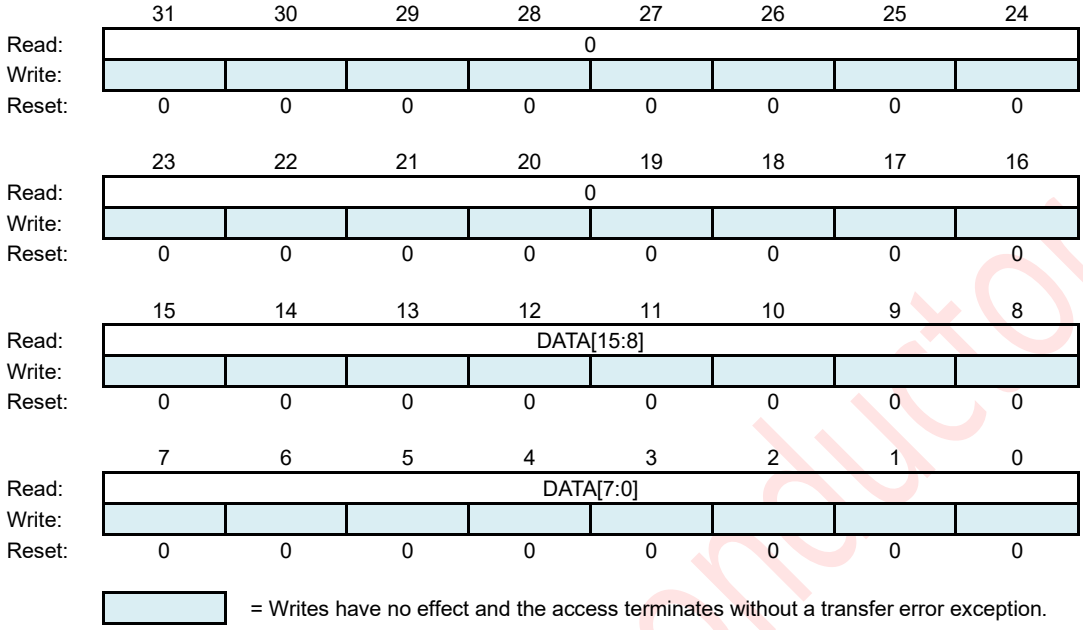


Figure 25-21: ADC FIFO Access Register (ADC_FIFO)

Read: Anytime

Write: Never

DATA[15:0] — Converted data

Refer to **Table 25-4.**

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26. TFT LCD Controller's Registers

The TFT LCD display controller is controlled by an internal 32-bit MCU, but it reserves 2 PWM and several IO ports for users to use as an extension of the MCU interface. It is usually only used for secondary development of LT7589, and users need to control these interfaces through these registers. The method of reading and writing registers can refer to the program code provided by Levetop Semiconductor.

26.1. PWM Control Register

REG[84h] PWM Prescaler Register (PSCLR)

Bit	Description	Default	Access
7-0	**PWM Prescaler Register** This register determine the pre-scaler value for Timer 0 and 1. The Base Frequency is: **Core_Freq / (Prescaler + 1)**	0	RW

REG[85h] PWM Clock Mux Register (PMUXR)

Bit	Description	Default	Access
7-6	**PWM Timer-1 (Select 2nd Clock Divider's MUX Input for PWM Timer-1)** 00b = 1 01b = 1/2 10b = 1/4 11b = 1/8	0	RW
5-4	**PWM Timer-0 (Select 2nd Clock Divider's MUX Input for PWM Timer-0)** 00b = 1 01b = 1/2 10b = 1/4 11b = 1/8	0	RW
3-2	**PWM[1] Function Control** 0xb: PWM[1] output system error flag (Scan FIFO POP error or Memory access out of range) 10b: PWM[1] output PWM timer 1 waveform or invert waveform of PWM timer 0 (dead zone enable) 11b: PWM[1] output Oscillator Clock If TEST[0] = 1, PWM[1] will be the input of the panel scanning frequency.	0	RW

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1-0	**PWM[0] Function Control** 0xb: PWM[0] becomes GPIO-C[7] 10b: PWM[0] output PWM Timer 0 11b: PWM[0] output Core Clock (CCLK)	0	RW

REG[86h] PWM Configuration Register (PCFGR)

Bit	Description	Default	Access
7	Reserved -- The value must be 0	0	RW
6	**PWM Timer-1 Output Inverter On/Off** Determine the output inverter to be On or Off for PWM1. 0 = Inverter off 1 = Inverter on for PWM1	0	RW
5	**PWM Timer-1 Auto Reload On/Off** Determine auto reload on/off for Timer 1. 0: One-Shot Mode 1: Interval Mode (Auto Reload)	1	RW
4	**PWM Timer-1 Start/Stop** 0: Stop 1: Start In Interval Mode, the MCU needs to program it as 0 to stop PWM timer. In One-shot Mode, this bit will be auto cleared. The MCU may read this bit to find out if the current PWMx is running or stopped.	0	RW
3	**PWM Timer-0 Dead Zone Enable** 0: Disable 1: Enable	0	RW
2	**PWM Timer-0 Output Inverter On/Off** Determine the output inverter to be On or Off for PWM0. 0 = Inverter off 1 = Inverter on for PWM0	0	RW
1	**PWM Timer-0 Auto Reload On/Off** Determine auto reload on/off for Timer 0. 0: One-Shot Mode 1: Interval Mode (Auto Reload)	1	RW
0	**PWM Timer-0 Start/Stop** 0: Stop	0	RW

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Bit	Description	Default	Access
	1: Start In Interval Mode, the MCU needs to program it as 0 to stop PWM timer. In One-shot Mode, this bit will be auto cleared. The MCU may read this bit to find out if the current PWMx is running or stopped.		

REG[87h] Timer-0 Dead Zone Length Register [DZ_LENGTH]

Bit	Description	Default	Access
7-0	**Timer-0 Dead Zone Length Register** These 8 bits determine the dead zone length. One unit time of the dead zone length is equal to one complete counting cycle of Timer 0.	0	RW

REG[89h-88h] Timer-0 Compare Buffer Register [TCMPB0]

Bit	Description	Default	Access
15-0	**Timer-0 compare Buffer Register** REG[89h] mapping to TCMPB0 [15:8]。 REG[88h] mapping to TCMPB0 [7:0]。 The Timer-0 Compare Buffer Registers have a total of 16bits. When the counter value is equal to or less than the value of this register, and the output inverter of PWM0 is off, then PWM0 output is high level.	0	RW

REG[8Bh-8Ah] Timer-0 Count Buffer Register [TCNTB0]

Bit	Description	Default	Access
15-0	**Timer-0 Count Buffer Register [15:0]** REG[8Bh] mapping to TCNTB0 [15:8] REG[8Ah] mapping to TCNTB0 [7:0] The Timer-0 count registers have a total of 16bit. When the counter is equal to 0 and the Reload_EN is enabled, the PWM will reload the value of this register to the counter. When the PWM begins to count, the current count value can be read back through this register.	0	RW

REG[8Dh-8Ch] Timer-1 Compare Buffer Register [TCMPB1]

Bit	Description	Default	Access

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15-0	**Timer-1 compare Buffer Register** REG[8Dh] mapping to TCMPB1 [15:8] REG[8Ch] mapping to TCMPB1 [7:0] The Timer-1 Compare Buffer Registers have a total of 16bits. When the counter value is equal to or less than the value of this register, and the output inverter of PWM1 is off, then PWM1 output is high level.	0	RW

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REG[8Fh-8Eh] Timer-1 Count Buffer Register [TCNTB1]

Bit	Description	Default	Access
15-0	**Timer-1 Count Buffer Register [15:0]** REG[8Fh] mapping to TCNTB1 [15:8]。 REG[8Eh] mapping to TCNTB1 [7:0]。 The Timer-1 count registers have a total of 16bit. When the counter is equal to 0 and the Reload_EN is enabled, the PWM will reload the value of this register to the counter. When the PWM begins to count, the current count value can be read back through this register.	0	RW

26.2. GPIO Register

REG[F0h] LCD_IOA Direction（LCD_IOADIR）

Bit	Description	Default	Access
7-2	**LCD_IOA[7:2] In/Out Control** 0: Output 1: Input	FFh	RW
1-0	Reserved	--	--

REG[F1h] LCD_IOA（LCD_IOA）

Bit	Description	Default	Access
7-2	**LCD_IOA[7:2] Data** Write: Set the output data of LCD_IOA. Read: Read input data from LCD_IOA. LCD_IOA [7:2] is a general-purpose I/O, and these pins can only be used with LT7589B.	NA	RW
1-0	Reserved	--	--

REG[F3h] GPIO-C Direction（GPIOCD）

Bit	Description	Default	Access
7	**GPIOC[7] In/Out Control** 0: Output 1: Input	FFh	RW
6-0	Reserved		

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REG[F4h] GPIO-C（GPIOC）

Bit	Description	Default	Access
7	**GPIOC[7] GPIOC[7] Data** Write: Set the output data of GPOC [7]. Read: Read input data from GPOC [7]. Note: The output data of GPOC [7] shares pins with PWM[0]. The GPOC function can only be used when the PWM and SPI Master functions of the TFT LCD controller are disabled.	NA	RW
6-0	Reserved	NA	RW

REG[F5h] GPIO-D Direction（GPIODD）

Bit	Description	Default	Access
7-0	**GPIO-D In/Out Control** 0: Output 1: Input	FFh	RW

REG[F6h] GPIO-D（GPIOD）

Bit	Description	Default	Access
7-0	**GPIO-D Data** Write： Set the output data for GPIOD [7:0]. Read： Read input data from GPOD [7:0]. GPOD [7:0] shares pins with PD [18, 2, 17, 16, 9, 8, 1, 0] . GPOD can only be used when the TFT LCD panel data bus is set to 16 bits (RGB: 565) . GPOD [7,6,3,2] can only be used when the LCD panel data bus is set to 16 bits.	NA	RW

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27. Electrical Characteristics

27.1. Absolute Maximum Ratings

Table 27-1: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD33}	Supply Voltage Range	-0.3 ~ 4.0	V
V_{IN}	Input Voltage Range	-0.3 ~ VDD33+0.3	V
V_{OUT}	Output Voltage Range	-0.3 ~ VDD33+0.3	V
P_D	Power Dissipation	≦300	mW
T_{OPR}	Operation Temperature Range (@120MHz)	-40 ~ 85	℃
T_{JT}	Junction Temperature Range	-40 ~ 105	℃
T_{ST}	Storage Temperature	-40 ~ 125	℃
T_{SOL}	Soldering Temperature	260	℃

Note:

If used beyond the absolute maximum ratings, LT7589 may be permanently damaged. It is strongly recommended that the device is used within the electrical characteristics. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device. This specification does not guarantee the accuracy of the parameters without a given upper and lower limit value, but it's typical value reasonably reflects the device performance.

27.2. DC Electrical Parameter

Table 27-2: DC Electrical Parameter

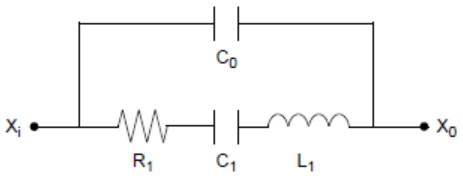
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD33} , V_{DD33_IO}	System Voltage		3.0	3.3	3.6	V
C_{VDD}	Loading Capacitor		1	-	10	uF
I_{OPR}	Operation Current	Note 1		60		mA
I_{STB}	Standby Mode	Note 1		30		mA
I_{SUSP}	Suspend Mode	Note 1		10		mA
I_{SLP}	Sleep Mode	Note 1		7		mA
T_{RMP}	Power Ramp Up Time	VDD Ramp Up to 3.3 V			35	ms
Oscillator Clock and PLL						
F_{OSC}	X'tal Oscillator Frequency	V_{DD33} = 3.3 V, Note 2		12		MHz
F_{VCO}	VCO Output Frequency		100		500	MHz
T_{LOCK}	Lock Time	Note 3			500	us
CLK_{MPLL}	MPLL Output Frequency (MCLK)	V_{DD33} = 3.3 V			133	MHz
CLK_{CPLL}	CPLL Output Frequency (CCLK)	V_{DD33} = 3.3 V			100	MHz
CLK_{PPLL}	PPLL Output Frequency (PCLK)	V_{DD33} = 3.3 V			80	MHz

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Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Serial Host Interface						
CLK_{SPI}	SPI Input Frequency				50	MHz
Input/Output (CMOS 3-State Output pad with Schmitt Trigger Input, Pull-Up/Down)						
V_{IH}	Input High Voltage		2		3.6	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{OH}	Output High Voltage		2.4			V
V_{OL}	Output Low Voltage				0.4	V
R_{PU}	Pull up Resistance		33	41	62	KΩ
R_{PD}	Pull down Resistance		33	42	68	KΩ
V_{TP}	Schmitt Trigger Low to High Threshold		1.5		2.1	V
V_{TN}	Schmitt Trigger High to Low Threshold		0.8		1.3	V
V_{HVS}	Hysteresis Voltage		200			mV
I_{LEAK}	Input Leakage Current		-10		+10	μA
V_{SLEW}	Rise/Fall Slew Rate			1.5		V/ns

(Condition: V_{DD} = 3.3V, T_A = 25℃)

Note 1:Test with serial SPI interface without additional loading.
Note 2: Parasitic capacitance effect when using crystal oscillator.



Standard Value: R1 = 50Ω (25-100Ω), L1 = 3.4mH, C1 = 13fF, C0 = 2.8pF

Figure 27-1: Equivalent Circuit Diagram Of Crystal Oscillator

Note 3: The time required from power startup to stable clock output of the internal PLL.

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Table 27-3: Power Characteristics

Items	Symbol	Min.	Typ.	Max.	Unit
Chip Power	VDD33A	2.97	3.3	3.63	V
	VDD33B	2.97	3.3	3.63	V
	VDD33_IO	2.97	3.3	3.63	V
ADC Power	AVDD	2.97	3.3	3.63	V
MCU Core Power (LDO O/P)	VDD12	1.1	1.2	1.3	V
LCD Controller Core Power (LDO O/P)	LCD_V12	1.1	1.2	1.3	V
RTC Battery Power	VBAT	2.7	3.3	3.6	V

Table 27-4: Thermal Characteristics

Symbol	Description	Range	Unit
RΘJC	Thermal Resistance: Junction to Case	3 ~ 8	℃/W
RΘJA	Thermal Resistance: Junction to Ambient	20 ~25	℃/W

27.3. ESD Protection

Table 27-5: ESD Protection

ESD Items	Symbol	Max.	Unit	Reference Standard
Human Body Model	HBM	4,000	V	ANSI/ESDA/JEDEC JS-001-2017
Machine Model	MM	200	V	JEDEC JESD22-A115C-2010
Charged Device Model	CDM	800	V	ANSI/ESDA/JEDEC JS-002-2022
Latch Up	LU	200	mA	JEDEC JESD78F.01-2022, @105℃

Note: When performing manual welding, it is recommended that personnel and equipment undergo anti-static treatment, such as appropriate temperature and humidity environment, welding equipment grounding, anti-static workbench, and welding personnel wearing anti-static wrist straps, etc.

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28. Package Information

28.1. LT7589A (QFN-96pin)

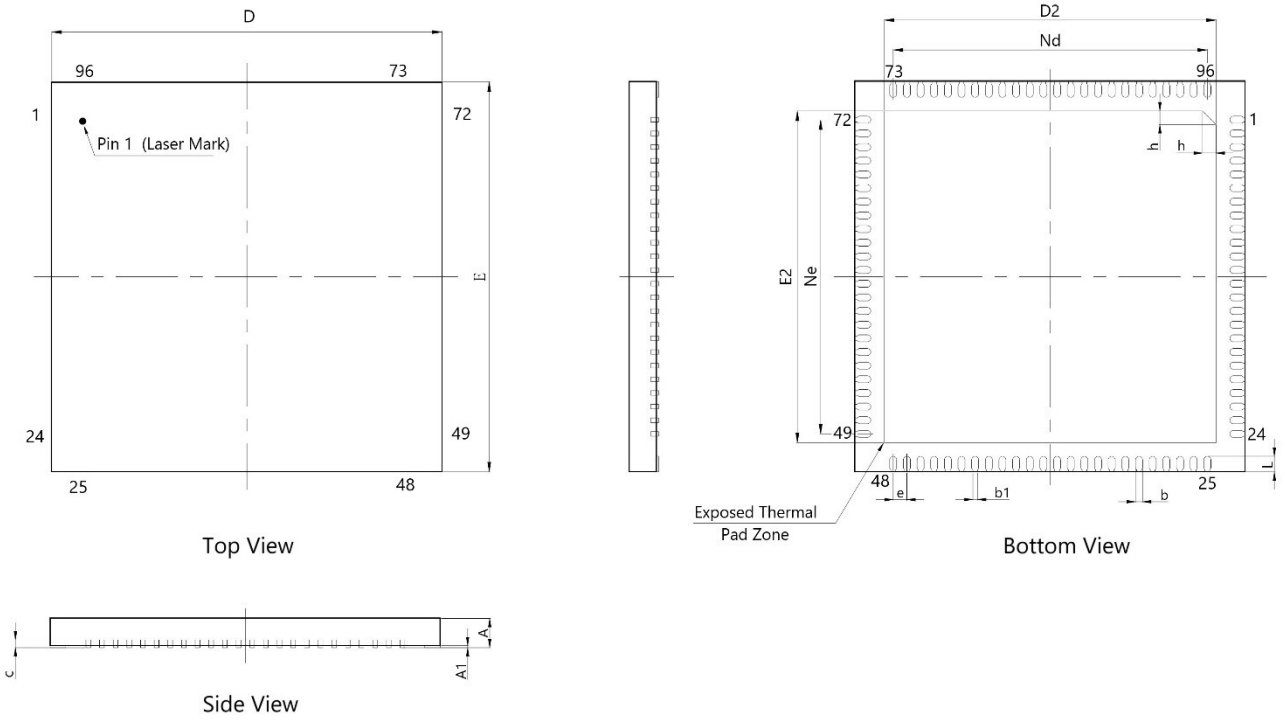


Figure 28-1: QFN-96Pin Outline

Note: When laying out the PCB, the thermal pad zone on the back of LT7589A must be directly grounded.

Table 28-1: QFN-96Pin Dimensions

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	0.80	0.85	0.9	E	9.90	10.00	10.10
A1	-	0.02	0.05	Ne	8.05BSC		
b	0.13	0.18	0.23	L	0.35	0.40	0.45
b1	0.12REF			E2	8.40	8.50	8.60
c	0.18	0.20	0.25	h	0.30	0.35	0.40
D	9.90	10.00	10.10	Nd	8.05BSC		
D2	8.40	8.50	8.60				
e	0.35BSC						

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28.2. LT7589B (LQFP-128pin)

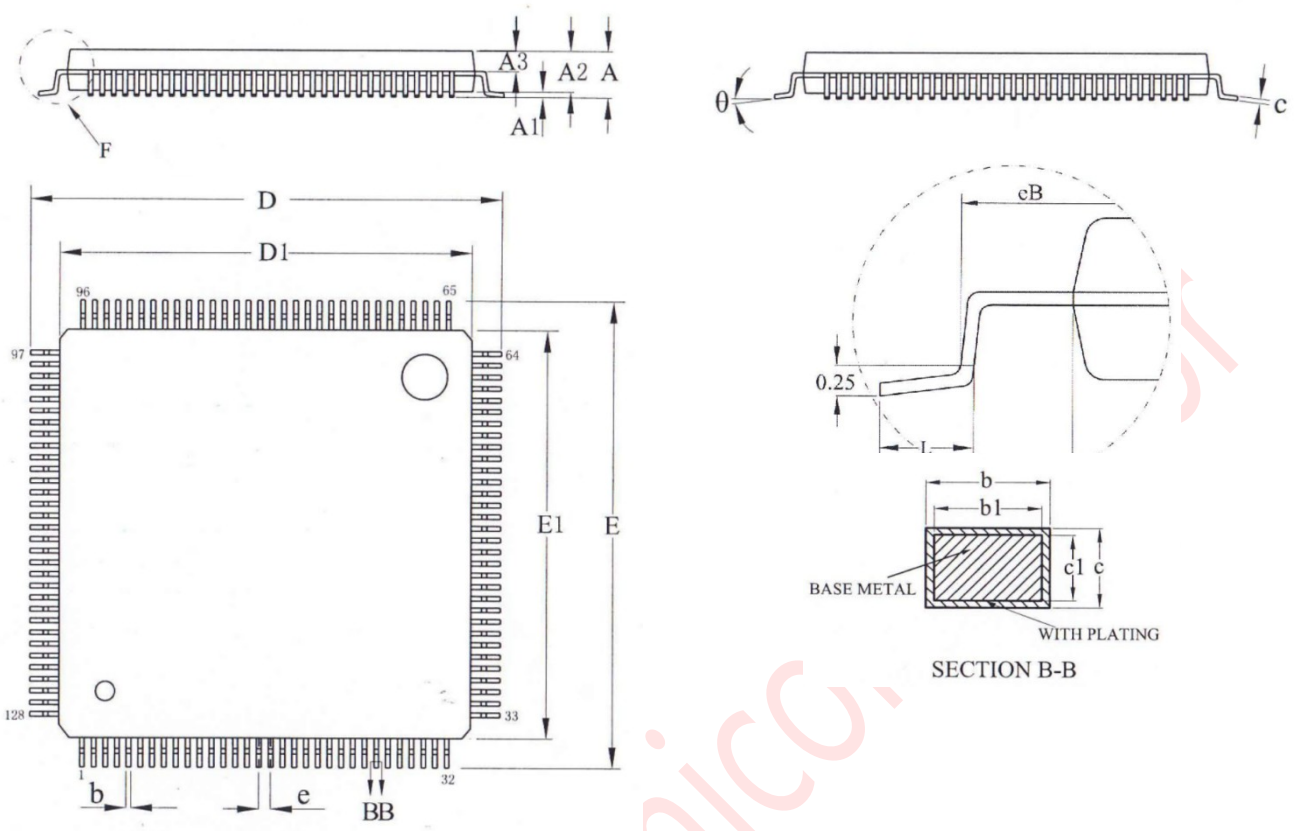


Figure 28-2: LQFP-128Pin Outline

Table 28-2: LQFP-128Pin Dimensions

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	-	-	1.60	**D1**	13.9	14.0	14.1
A1	0.05	-	0.15	**E**	15.8	16.0	16.2
A2	1.35	1.40	1.45	**E1**	13.9	14.0	14.1
A3	0.59	0.64	0.69	**eB**	15.05	-	15.35
b	0.14	-	0.22	**e**	0.40BSC		
b1	0.13	0.16	0.19	**L**	0.45	-	0.75
c	0.13	-	0.17	**L1**	1.00REF		
c1	0.12	0.13	0.14	**θ**	0		7
D	15.8	16.00	16.2				

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28.3. LT7589A PCB Layout Suggestions

LT7589A adopts QFN packaging, with ground (GND) heat dissipation pads on the back of the chip. In order to achieve better heat dissipation and reduce soldering risks, it is recommended to divide the PCB copper foil surface of the bottom solder pad of LT7589A into four or more small solder surfaces (square or circular) during PCB layout, and set the interval between each solder surface to~0.8mm to avoid incomplete soldering caused by the use of complete solder surfaces with the same or even larger size than LT7589A solder pads, or chip deformation and poor contact caused by PCB and chip solder pad pulling after solder cooling. The correct PCB pad layout is shown in the following two examples of LT7589A. The light-yellow area in the middle is the grounding pad at the bottom of LT7589A, and the gray area is the PCB grounding small pad (welding surface). Each pad can be grounded 1-2 times through a through-hole.

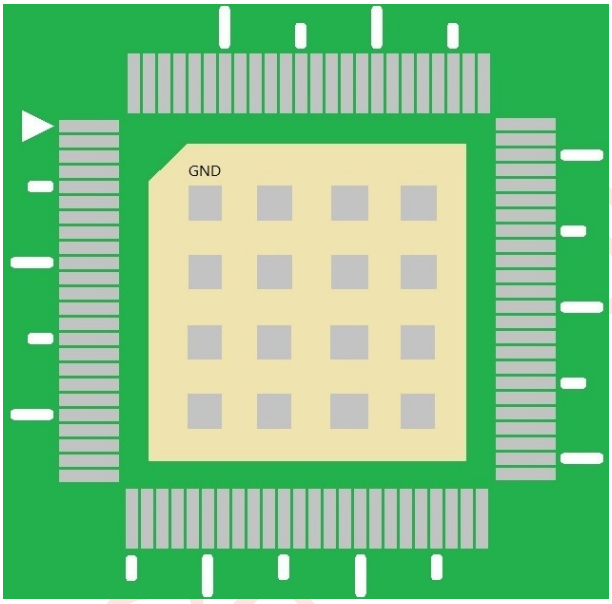


Figure 28-3: Design Suggestion-1 for LT7589A Bottom Pad PCB Layout

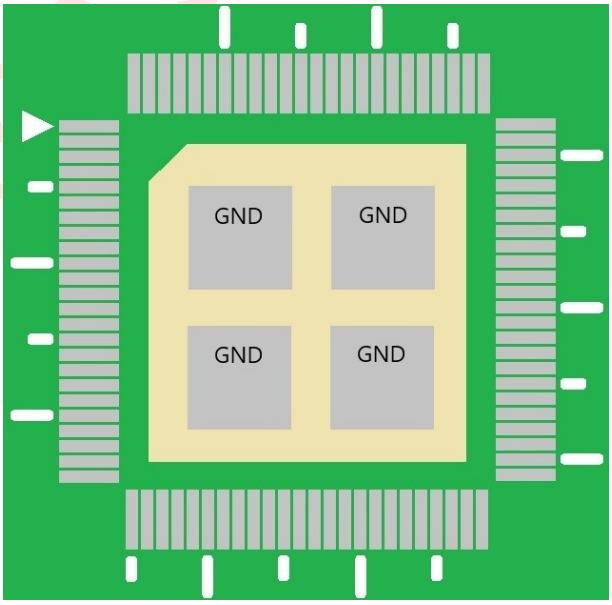


Figure 28-4: Design Suggestion-2 for LT7589A Bottom Pad PCB Layout

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29. Application Circuit

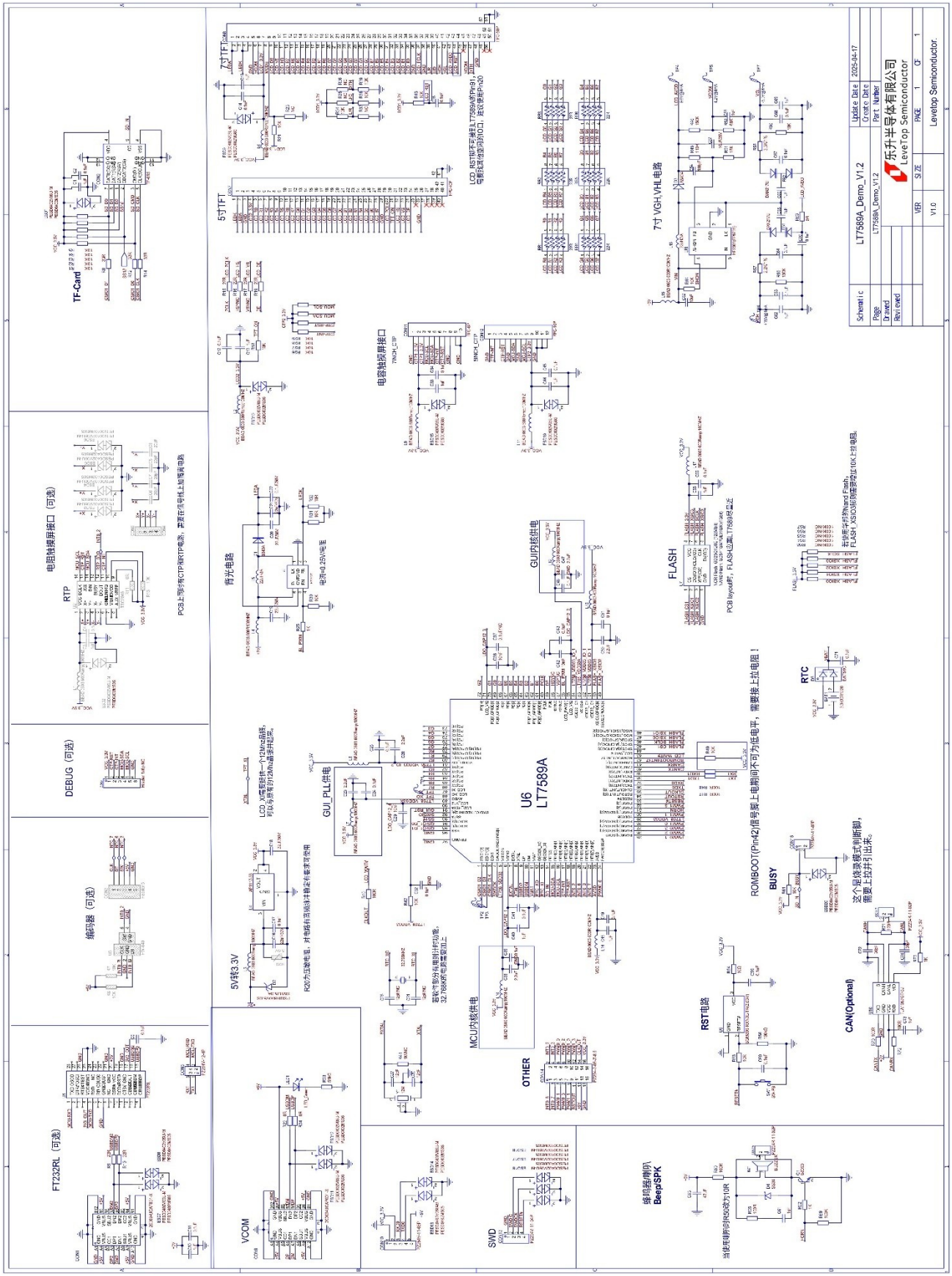


Figure 29-1: LT7589A Application Circuit

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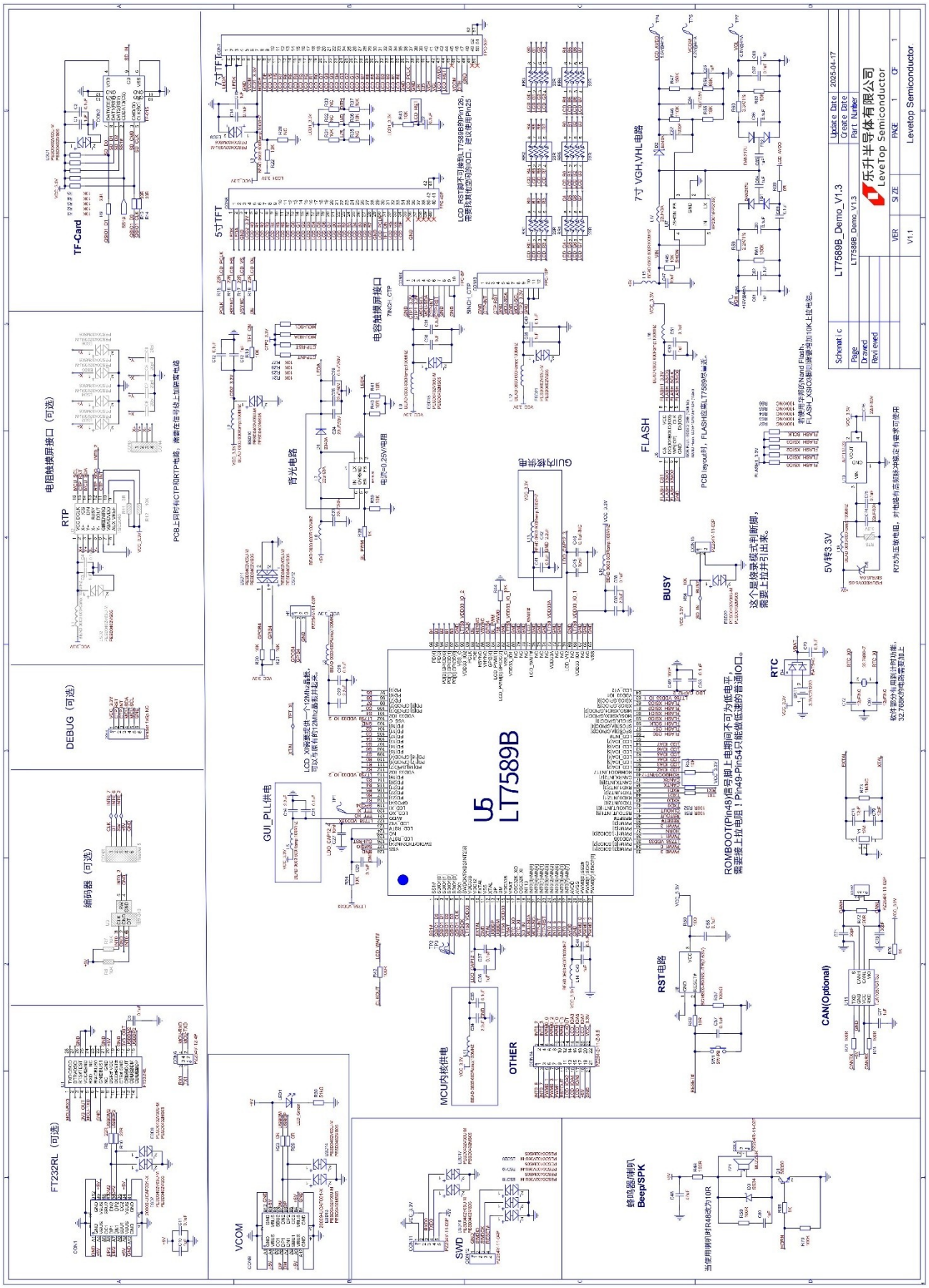


Figure 29-2: LT7589B Application Circuit

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